A High-Speed CMOS Comparator for Use in an ADC

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Abstract—**A high-speed CMOS comparator has been designed and fabricated using a standard 3-μm process. A dynamic latch preceded by an offset-cancelled amplifier is used to obtain a response time of 43 ns. The offset-cancelled amplifier reduces the input-referred offset so that medium-resolution analog-to-digital converters (ADC's) can be built with this comparator. The use of pipelining within the comparator enables the offset cancellation to be done as the dynamic latch is enabled. Finally, power and area are optimally distributed within the amplifier to minimize response time.**

I. Introduction

SEVERAL analog-to-digital converters (ADC's) have recently been reported that operate at sampling frequencies between 200 and 400 MHz [1]–[3]. However, the fastest 8-bit CMOS ADC can sample up to only 25 MHz [4]. CMOS flash ADC's, with their cost-effectiveness and VLSI logic compatibility, are well suited for use in the growing field of digital video-signal processing.

In a flash ADC, internal comparators must amplify small voltages into logic levels. Once the result is stored into a latch, logic is enabled to encode the outputs of the 2^N-1 comparators into N bits. Depending on the algorithm used, encoding process can often be pipelined with the comparator function. Since the encoding process is faster than the comparator function, the maximum conversion rate for the ADC is limited by the response time of its comparators. Therefore, the design and optimization of the comparators is critically important.

The comparator architecture consists of dynamic latch preceded by an offset-cancelled amplifier. The positive feedback of the dynamic latch is used to efficiently charge and discharge the comparator output nodes. The offset-cancelled amplifier reduces the input-referred offset so that medium-resolution ADC's are possible. The use of pipelining within the comparator enables the offset cancellation to begin as the dynamic latch is enabled. Power and area are optimally distributed within the amplifier so that the comparator response time is minimized.

Section II deals with the comparator topology where power and area constraints, the motivation for offset cancellation, and the amplifier and dynamic latch optimizations are discussed. Section III describes the device-level circuit design of the amplifier and dynamic latch. Section IV presents the experimental results from a single 3-μm CMOS comparator designed and fabricated to verify the architecture.

II. Choice of Topology

A. Comparator Constraints

When designing an N-bit flash ADC, 2^N-1 comparators are required. For medium-resolution ADC's, the amount of power and area consumed per comparator is of the utmost importance. Therefore, when evaluating different comparator topologies for use in a flash ADC, the amount of power and area consumed must be held constant. Assume initially that a single-stage amplifier is compared to a two-stage amplifier. The single-stage amplifier draws I current and uses A area. The two-stage amplifier draws I_1+I_2 current and uses A_1+A_2 area where the 1 and 2 subscripts designate the first and second stage, respectively. Therefore

$$I_1+I_2=I \tag{1}$$

$$A_1+A_2=A. \tag{2}$$

Since designing high-speed circuits is the ultimate goal, it is assumed that the channel length L is held at a minimum and that the area is controlled by the device width W. Therefore, (2) becomes

$$W_1+W_2=W. \tag{3}$$

In order to maintain constant node voltages, as the current in stage one of the two-stage amplifier increases, the channel width must also increase. Thus

$$\frac{I_1}{W_1}=\frac{I_2}{W_2}. \tag{4}$$

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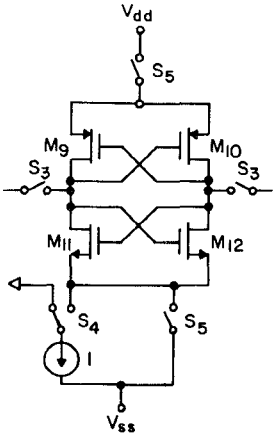

Fig. 1. The dynamic latch.

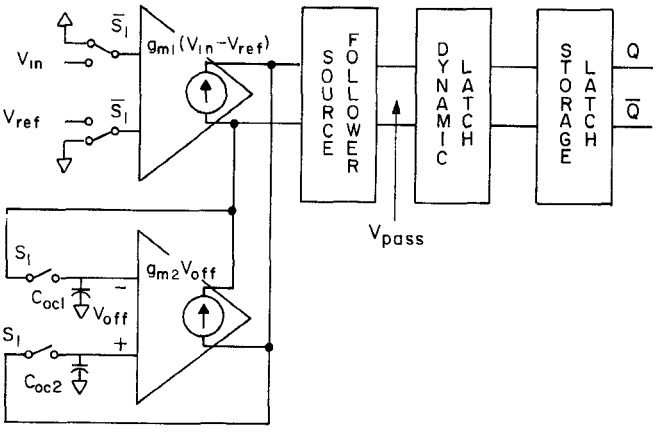

Fig. 2. The comparator block diagram.

The transconductance is given by $g_m = \sqrt{2\mu C_{ox} I(W/L)}$. Therefore

$$(g_{m_1} + g_{m_2})^2 = \frac{2\mu C_{ox}}{L}\left(W_1 I_1 + W_2 I_2 + 2\sqrt{W_1 I_1 W_2 I_2}\right)$$

$$= \frac{2\mu C_{ox}}{L}(W_1 I_1 + W_2 I_2 + W_1 I_2 + W_2 I_1)$$

$$= \frac{2\mu C_{ox}}{L}(W_1 + W_2)(I_1 + I_2).$$

Thus

$$(g_{m_1} + g_{m_2})^2 = G_m^2. \tag{5}$$

Equation (5) shows that if the total power and area are held constant, the total transconductance is also constant.

B. Comparator Architecture

The dynamic latch (Fig. 1), often used as a sense amplifier in dynamic RAM's, is a fast CMOS comparator. However, its large offset voltage limits its resolution to about 5 bits. A linear amplifier may precede the dynamic latch so that the voltage applied to the latch is large enough to overcome this offset. Since a linear amplifier can be offset-cancelled, medium-resolution ($\approx$ 8-bit) converters are possible.

Fig. 2 shows the comparator block diagram, which consists of a dynamic latch preceded by an offset-cancelled amplifier [5]. The offset-cancellation cycle begins by throwing the switch $\overline{S_1}$ to ground and closing the switch S_1. The offset-cancellation amplifier (g_{m2}) forces its offset (V_{os2}) and the offset (V_{os1}) from the high-gain amplifier (g_{m_1}) onto the offset-cancellation capacitors C_{oc1} and C_{oc2}. This voltage V_{off} is given by

$$V_{\text{off}} = \frac{R_L(g_{m1}V_{os1} + g_{m2}V_{os2})}{1 + g_{m2}R_L}. \tag{6}$$

The input-referred offset voltage V_{os} is reduced by the voltage gain of the high-gain amplifier and is given by

$$V_{os} = \frac{R_L(g_{m1}V_{os1} + g_{m2}V_{os2})}{g_{m1}R_L(1 + g_{m2}R_L)}. \tag{7}$$

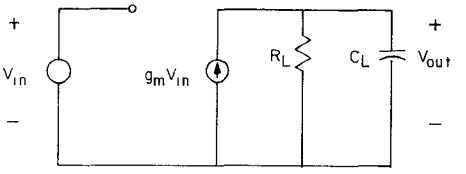

Fig. 3. A one-stage single-pole amplifier.

The amplify cycle begins by throwing the switch $\overline{S_1}$ to sample the input voltage and opening the switch S_1. Now, the amplifier output voltage V_{pass} is a rising exponential whose final value is the product of $V_{\text{in}} - V_{\text{ref}}$ and the voltage gain $g_{m1}R_L$.

Once the voltage V_{pass} is large enough (about 50 mV), the dynamic latch is enabled. Since it has positive feedback, it is able to "amplify" the pass voltage to near logic levels in a short period of time. Then the storage latch is turned on to hold the result until the encode logic is enabled.

C. Motivation for Offset Cancellation

The initial motivation for offset cancellation is clear: without it, an MOS comparator could not resolve small enough voltages so that it could be used in a medium-resolution ADC. Since it takes a finite amount of time to complete the offset-cancellation cycle before the comparator can be enabled, it seems that the comparator response time must be increased. However, if the offset-cancellation cycle is pipelined with the dynamic latch cycle, it does not degrade the response time.

Consider the simple one-stage, single-pole amplifier shown in Fig. 3. The step response for the amplifier is given by

$$V_{\text{out}}(t) = \left[g_m R_L V_{\text{in}}(0_+)(1 - e^{-t/R_L C_L}) + V_{\text{out}}(0)e^{-t/R_L C_L}\right]u(t). \tag{8}$$

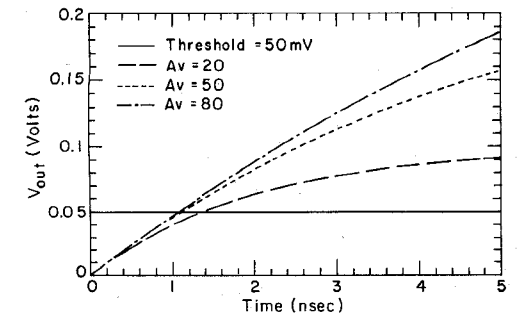

Fig. 4. (a) One-stage amplifier step response for $V_{out}(0) = 0$. (b) One-stage amplifier step response for $V_{out}(0) = -0.15$ V.

The first term is a rising exponential with the magnitude determined by the voltage gain $g_m R_L$ times the input step $V_{in}(0_+)$. The second term is just the exponential decay of the residual voltage from the last comparison $V_{out}(0)$.

Consider the one-stage amplifier for two cases. First, assume that the initial output voltage $V_{out}(0)$ is zero and that the following conditions hold: $g_m = 0.001$ S, $C_L = 100$ fF, $V_{in}(0_+) = 5$ mV, and that the voltage gain is varied from 20 to 80 by adjusting R_L. The result is shown in Fig. 4(a). For any time t, the highest-gain configuration has "amplified" the 5-mV input voltage into the largest output voltage. For small t, the slope of the step response for each configuration is given by g_m/C_L so that the response time can be improved by increasing g_m or decreasing C_L and is independent of R_L (only for $t \ll R_L C_L$).

Now, assume that the same conditions hold as above except that $V_{out}(0) = -0.15$ V. Due to the decaying residual voltage from the last sample, the high-gain amplifier is no longer the best choice. In fact, the lowest-gain amplifier reaches the 50-mV threshold before the other configurations in this example (Fig. 4(b)), and the "best" choice is highly dependent on this residual voltage. However, if this residual output voltage is nulled in an offset-cancellation cycle as in the first example, the high-gain amplifier is always optimum. Therefore, a high-gain amplifier with offset cancellation is used in designing the flash ADC comparator.

D. Amplifier Optimization

Our goal is to determine how the power and area should be distributed throughout the amplifier in order to minimize the comparator response time. We begin by determining the optimization for three different amplifier configurations: single-stage, single-stage plus source follower, and two-stage plus source follower. The results can be extended to higher-order amplifiers.

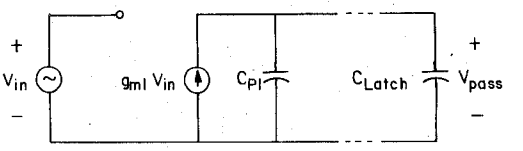

Fig. 5. Single-stage amplifier driving the dynamic latch.

1. Single-Stage Amplifier: Consider the single-stage amplifier shown in Fig. 5. A transconductance amplifier g_{m1} drives the input capacitance of the latch C_{Latch} and the parasitic capacitance C_{p1}. If the output voltage V_{pass} is nulled before the amplify cycle, the output voltage is given by

$$V_{pass} = \frac{V_{in} g_{m1} t}{C_{p1} + C_{Latch}} u(t) \tag{9}$$

and the time delay t_d to reach a desired pass voltage is

$$t_d = \frac{V_{pass}}{v_{in}} \frac{C_{p1} + C_{Latch}}{g_{m1}}. \tag{10}$$

The offset-cancellation time constant is given by

$$\tau = \frac{C_{p1} + C_{oc}}{g_{m2}} \tag{11}$$

where C_{oc} is the offset-cancellation hold capacitance and g_{m2} is the offset-cancellation amplifier transconductance. The total comparator response time t_r is then

$$t_r = \frac{V_{pass}}{V_{in}} \frac{C_{p1} + C_{Latch}}{g_{m1}} + M \frac{C_{p1} + C_{oc}}{g_{m2}} \tag{12}$$

where M is the number of time constants used to perform the offset cancellation. Due to the power and area constraints, $g_{m1} + g_{m2} = G_m$. The partial derivative of t_r with respect to g_{m1} can be taken and set equal to zero to determine the minimum comparator response time:

$$\frac{\partial t_r}{\partial g_{m1}} = -\frac{V_{pass}}{V_{in}} \frac{C_{p1} + C_{Latch}}{g_{m1}^2} + M \frac{C_{p1} + C_{oc}}{(G_m - g_{m1})^2} = 0. \tag{13}$$

Solving (13) for g_{m1} gives

$$g_{m1} = \frac{G_m \sqrt{\frac{V_{pass}}{V_{in}} (C_{p1} + C_{Latch})}}{\sqrt{M(C_{p1} + C_{oc})} + \sqrt{\frac{V_{pass}}{V_{in}} (C_{p1} + C_{Latch})}}. \tag{14}$$

The optimum comparator response time can now be determined for a given power and area constraint.

2. Single-Stage Amplifier Plus Source Follower: By adding a source follower, the latch capacitance is buffered from the high-gain amplifier at the expense of adding some group delay. Also, the source follower has the added benefit of buffering the high-gain amplifier from the kickback charge of the dynamic latch.

The step response for the single-stage amplifier plus source follower is approximated by

$$V_{\text{pass}} \approx \frac{V_{\text{in}} g_{m1}}{C_{p1}} \left(t - \frac{C_{\text{Latch}}}{g_{m3}} \right) u(t) \tag{15}$$

where g_{m3} is the source-follower transconductance. The time delay is thus

$$t_d = \frac{V_{\text{pass}}}{V_{\text{in}}} \frac{C_{p1}}{g_{m1}} + \frac{C_{\text{Latch}}}{g_{m3}} \tag{16}$$

and the comparator response time is given by

$$t_r = \frac{V_{\text{pass}}}{V_{\text{in}}} \frac{C_{p1}}{g_{m1}} + \frac{C_{\text{Latch}}}{g_{m3}} + M \frac{C_{p1} + C_{oc}}{g_{m2}}. \tag{17}$$

Since the total transconductance G_m must be held constant, then $g_{m3} = G_m - g_{m1} - g_{m2}$. Therefore, (17) becomes

$$t_r = \frac{V_{\text{pass}}}{V_{\text{in}}} \frac{C_{p1}}{g_{m1}} + \frac{C_{\text{Latch}}}{G_m - g_{m1} - g_{m2}} + M \frac{C_{p1} + C_{oc}}{g_{m2}}. \tag{18}$$

By taking separate partial derivatives of (18) with respect to g_{m1} and g_{m2} and setting them equal to zero, the following relationship results:

$$g_{m1} = g_{m2} \sqrt{\frac{V_{\text{pass}}}{V_{\text{in}}} \frac{C_{p1}}{M(C_{p1} + C_{oc})}}. \tag{19}$$

In order to determine the relationship between g_{m3} and g_{m2}, substitute $g_{m1} = G_m - g_{m2} - g_{m3}$ into (17). Then take separate partial derivatives of t_r with respect to g_{m3} and g_{m2} and set them both equal to zero. Solving this result gives

$$g_{m3} = g_{m2} \sqrt{\frac{C_{\text{Latch}}}{M(C_{p1} + C_{oc})}}. \tag{20}$$

By taking (19), (20), and remembering that $g_{m1} + g_{m2} + g_{m3} = G_m$, the three individual transconductances can be determined in terms of G_m. Thus

$$g_{m1} = \frac{G_m \sqrt{\frac{V_{\text{pass}}}{V_{\text{in}}} \frac{C_{p1}}{M(C_{p1} + C_{oc})}}}{1 + \sqrt{\frac{V_{\text{pass}}}{V_{\text{in}}} \frac{C_{p1}}{M(C_{p1} + C_{oc})}} + \sqrt{\frac{C_{\text{Latch}}}{M(C_{p1} + C_{oc})}}} \tag{21}$$

$$g_{m2} = \frac{G_m}{1 + \sqrt{\frac{V_{\text{pass}}}{V_{\text{in}}} \frac{C_{p1}}{M(C_{p1} + C_{oc})}} + \sqrt{\frac{C_{\text{Latch}}}{M(C_{p1} + C_{oc})}}} \tag{22}$$

$$g_{m3} = \frac{G_m \sqrt{\frac{C_{\text{Latch}}}{M(C_{p1} + C_{oc})}}}{1 + \sqrt{\frac{V_{\text{pass}}}{V_{\text{in}}} \frac{C_{p1}}{M(C_{p1} + C_{oc})}} + \sqrt{\frac{C_{\text{Latch}}}{M(C_{p1} + C_{oc})}}}. \tag{23}$$

Once the optimum transconductances are known, they can be substituted back into (17) to determine the optimum comparator response time for the single-stage plus source-follower configuration.

3. Two-Stage Amplifier Plus Source Follower: Taking this a step further, consider two single-pole amplifier stages cascaded together and buffered by a source follower. The transconductance for the two gain stages must be divided by two in order to keep the total transconductance constant. If the parasitic capacitance C_{p1} is dominated by gate capacitance, it must also be divided by two. The resulting pass voltage can be approximated by

$$V_{\text{pass}} \approx \frac{V_{\text{in}}}{2} \left(\frac{g_{m1}}{C_{p1}} \right)^2 \left(t - \frac{C_{\text{Latch}}}{g_{m3}} \right)^2 u(t). \tag{24}$$

The time delay is

$$t_d = \sqrt{\frac{2V_{\text{pass}}}{V_{\text{in}}}} \left(\frac{C_{p1}}{g_{m1}} \right) + \frac{C_{\text{Latch}}}{g_{m3}}. \tag{25}$$

The comparator response time is given by

$$t_r = \sqrt{\frac{2V_{\text{pass}}}{V_{\text{in}}}} \left(\frac{C_{p1}}{g_{m1}} \right) + \frac{C_{\text{Latch}}}{g_{m3}} + M \frac{C_{p1} + C_{oc}}{g_{m2}}. \tag{26}$$

Note that (26) is the same as (17) with $V_{\text{pass}}/V_{\text{in}}$ replaced by $\sqrt{2V_{\text{pass}}/V_{\text{in}}}$. Therefore, the optimum transconductances can be determined by making the above substitution into (21)–(23). Then, these transconductances can be substituted into (26) to determine the optimum comparator response time for the two-stage plus source-follower configuration.

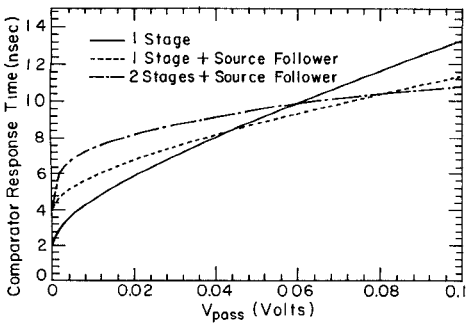

Fig. 6. Optimized comparator response time for three high-gain amplifier configurations for $C_{p1} = 200$ fF, $C_{Latch} = 300$ fF, $C_{oc} = 200$ fF, $V_{in} = 10$ mV, and $G_m = 1$ mS.

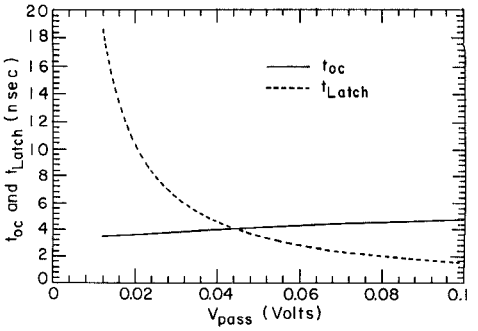

Fig. 7. Latch and offset-cancellation amplifier response times versus pass voltage for $C_{p1} = 200$ fF, $C_{Latch} = 300$ fF, $C_{oc} = 200$ fF, $V_{in} = 10$ mV, $G_m = 1$ mS, $W = 10$ μm, $L = 2$ μm, and $\Delta L = 0.1$ μm.

4. Amplifier Optimization Results: Fig. 6 shows the optimized time delay t_d versus pass voltage V_{pass} for the three amplifier configurations considered above. It is interesting to note that the fastest amplifier configuration depends on the desired pass voltage. For pass voltages between 0 and 45 mV, the single-stage amplifier is fastest; for pass voltages between 45 and 80 mV, the single-stage amplifier source follower is fastest; for pass voltages greater than 80 mV, the two-stage amplifier is fastest; etc. If a large pass voltage were desired or if the input voltage were smaller (it is 10 mV in this example) higher order amplifiers become optimum. For an 8-bit ADC with a dynamic range of 2.5 V, 10 mV corresponds to 1 LSB and, as will be shown in the next subsection, 50 mV is the optimum pass voltage. Therefore, the one-stage amplifier plus source follower is the optimum amplifier configuration.

E. Dynamic Latch Optimization

It was previously mentioned that the dynamic latch has a large offset voltage. Unlike the offset of the high-gain amplifier, it is difficult to cancel the dynamic latch offset. Therefore, it is important to understand the origin of this offset so that its effects can be minimized.

Consider the dynamic latch shown in Fig. 1. Assume that the initial voltage V_{pass} has been applied by closing and then opening S_3. The switches S_5 are initially opened and switch S_4 is thrown to the right. Since no current can flow through them, transistors M_9 and M_{10} are initially off. Either or both transistors M_{11} and M_{12} are on and the small-signal voltage across their gates is given by

$$V_{out} = (V_{pass} - V_{os}) e^{t g_{m_{Latch}}/C_{Latch}} \tag{27}$$

where the offset voltage V_{os} is assumed to oppose the pass voltage V_{pass}. The dynamic latch response time t_{Latch} is given by

$$t_{Latch} = \frac{C_L}{g_{m_{Latch}}} \ln\left(\frac{V_{out}}{V_{pass} - V_{os}}\right). \tag{28}$$

Using the square law approximation for an MOS transistor $I_d = K(V_{gs} - V_t)^2$ where $K = (\mu C_{ox}/2)(W/L)$ the offset voltage is given by

$$V_{os} = \Delta V_t + \frac{I \Delta K}{g_{m_{Latch}} K} = \Delta V_t + \frac{g_{m_{Latch}} \Delta K}{4K^2}. \tag{29}$$

By taking the partial derivative of t_{Latch} with respect to $g_{m_{Latch}}$ and setting it equal to zero, the optimum response time for a dynamic latch with a worst-case opposing offset voltage can be determined:

$$\frac{\partial t_{Latch}}{\partial g_{m_{Latch}}} = \frac{C_{Latch}}{g_{m_{Latch}}} \frac{1}{V_{pass} - V_{os}} \frac{\partial V_{os}}{\partial g_{m_{Latch}}} - \frac{C_{Latch}}{g^2_{m_{Latch}}} \ln\left(\frac{V_{out}}{V_{pass} - V_{os}}\right) = 0. \tag{30}$$

Since from (29)

$$\frac{\partial V_{os}}{\partial g_{m_{Latch}}} = \frac{\Delta K}{4K^2} \tag{31}$$

and since

$$\frac{\Delta K}{K} = -\frac{\Delta L}{L} \tag{32}$$

(30) becomes

$$\frac{\partial t_{Latch}}{\partial g_{m_{Latch}}} = 0 = \frac{\Delta L}{4KL\left(V_{pass} - \Delta V_t - \dfrac{g_{m_{Latch}} \Delta L}{4KL}\right)} - \frac{1}{g_{m_{Latch}}} \ln\left(\frac{V_{out}}{V_{pass} - \Delta V_t - \dfrac{g_{m_{Latch}} \Delta L}{4KL}}\right). \tag{33}$$

Equation (33) can be solved iteratively for the optimum $g_{m_{Latch}}$, which can be substituted into (28) to obtain the optimum t_{Latch}. Since the dynamic latch-response time t_{Latch} must fit into the offset-cancellation time t_{oc}, the optimum pass voltage V_{pass} can be found by plotting the optimum t_{Latch} and t_{oc} with respect to V_{pass} and noting where they intersect. This is done in Fig. 7 for $V_{out} = 1$ V. An optimum pass voltage of 50 mV has been chosen in our design.

After a few nanoseconds, the switches S_5 are closed (Fig. 1) and the differential output of the dynamic latch quickly approaches logic levels. Then, the storage latch is enabled to hold the result.

III. Circuit Description

For an 8-bit flash ADC it has been shown that the optimum topology consists of a single-stage amplifier plus source follower, an offset-cancellation amplifier, a dynamic latch, and a storage latch as shown in Fig. 2. A detailed discussion of the circuit implementation of these blocks in now given.

Fig. 8 shows the high-gain amplifier plus source follower and the offset-cancellation amplifier. The differential pair consisting of transistors M_1 and M_2 constitutes the high-gain amplifier. Transistors M_5 and M_6 make up the offset-cancellation amplifier. Since the drains of M_1 and M_2 connect to the drains of M_5 and M_6, both the high-gain amplifier and the offset-cancellation amplifier are cascoded by transistors M_3 and M_4. This increases the output resistance of the amplifiers, thus increasing the voltage gain. It also reduces the Miller effect, thus improving the comparator response time. Transistors M_7 and M_8 are the source followers.

To insure that transistors M_1 through M_6 in the high gain and offset-cancellation amplifiers are all operating in the saturation region, a simple common-mode feedback circuit is employed. The high impedance nodes of each differential amplifier are tied to the gates of source followers. The output current of these two source followers is summed into a diode-connected transistor producing a voltage CMFB. This voltage is tied to the gate of the current source transistor for the differential pair. The sum of the currents from these source followers remains constant with a small signal differential voltage at the high impedance nodes. If a common mode voltage appears at the high impedance nodes, the sum of the source follower currents causes a change in voltage CMFB to return the common mode voltage near 0. This common mode feedback circuit has only one pole and therefore is unity gain stable without compensation. A more complete explanation of this circuit is discussed in [6].

The dynamic and storage latches are shown in Fig. 9. Transistors M_9 through M_{12} are the dynamic latch and transistors M_{13} through M_{16} make up the storage latch. The dynamic latch is first turned on slowly by throwing switch S_4 to the right. The current source I is chosen to establish the optimum $g_{m_{\text{Latch}}}$. After a few nanoseconds, the S_5 switches are closed to quickly bring the dynamic latch output near logic levels.

A tri-state inverter separates the two latches. It is enabled one-half of a cycle after the dynamic latch is enabled. Then, switches designated by S_6 are closed and the storage latch holds the result until the encode logic is enabled.

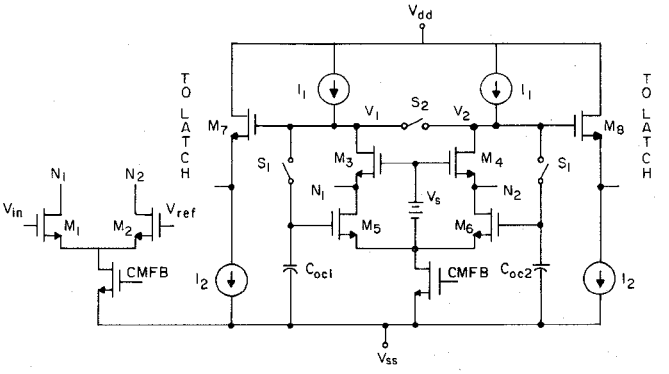

Fig. 8. Schematic diagrams of high-gain amplifier plus source follower and offset-cancellation amplifier.

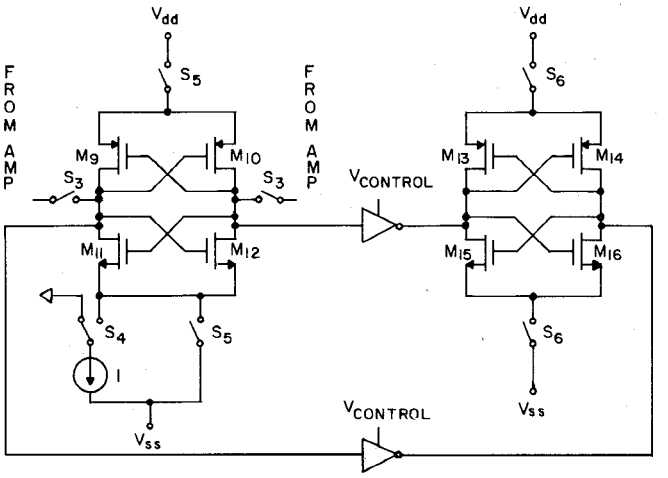

Fig. 9. Schematic of dynamic and storage latches.

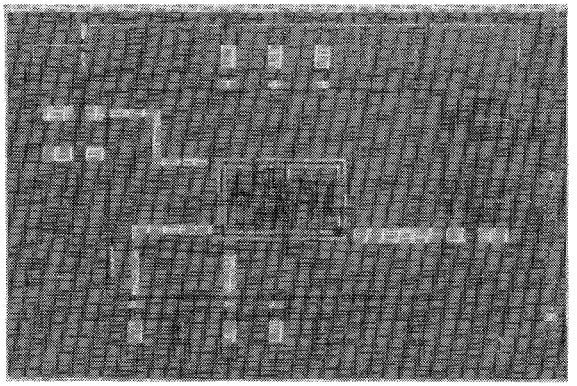

Fig. 10. Comparator die photo.

IV. Experimental Results

In order to verify the comparator architecture, a 3-μm CMOS comparator has been fabricated by MOSIS (see die photo in Fig. 10). Fig. 11 shows the comparator response (bottom trace) to a 900-mV peak-to-peak 1.44-MHz sine wave sampled at 23 MHz. Due to the time delay of the comparator, the storage latch, and the pad drivers, the comparator output lags the input sine wave. The results agree quite well with SPICE simulations that predict the 3-μm comparator will function up to 25 MHz.

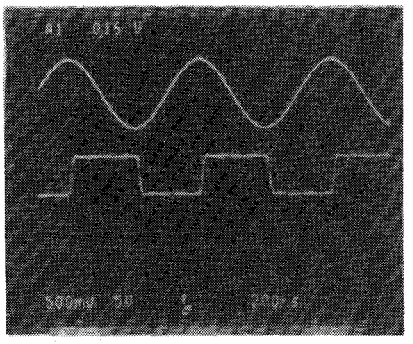

Fig. 11. Comparator response to a 1.44-MHz sine wave while being clocked at 23 MHz.

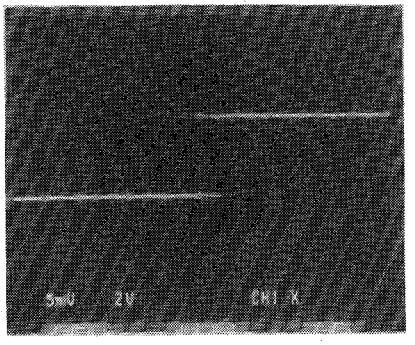

Fig. 12. Comparator noise and hysteresis while being clocked at 23 MHz.

Fig. 12 shows the comparator noise and hysteresis by applying a triangle wave to both the comparator input and the X axis of the oscilloscope. The 10-mV noise window is due mostly to clock feedthrough in a track and hold that precedes the comparator. Two complementary strobes are needed to control the track and hold. Since one is buffered on chip and the other is not, truly complementary strobes are not being applied internally.

A 2-μm CMOS flash ADC using the comparator architecture discussed here is being fabricated. The clock feedthrough in the track and hold is reduced by the use of on-chip clock generation. The 2-μm comparator used in the flash ADC has the dimensions 130 μm by 500 μm.

V. Conclusions

A CMOS comparator design and optimization procedure has been developed for use in an ADC. A dynamic latch preceded by an offset-cancelled amplifier has been used to build a fast and precise comparator. The use of pipelining within the comparator enabled the offset-cancellation and latch functions to be accomplished simultaneously. In addition, an optimal distribution of power and area within the amplifier was developed so that the comparator response time was minimized.

Using a 3-μm CMOS process, a single comparator has been built and tested. It operated at a minimum response time of 43.5 ns with a noise and hysteresis window of 10 mV that is limited by clock feedthrough in the input track and hold.

Acknowledgment

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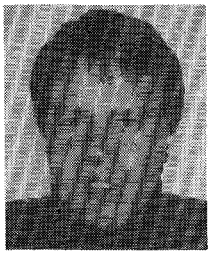

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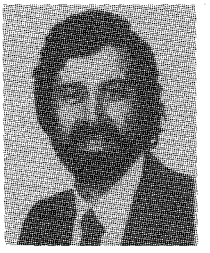

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