A Low-Power Reconfigurable Analog-to-Digital Converter

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***Abstract*—A low-power CMOS reconfigurable analog-to-digital converter that can digitize signals over a wide range of bandwidth and resolution with adaptive power consumption is described. The converter achieves the wide operating range by (1) reconfiguring its architecture between pipeline and delta–sigma modes; (2) varying its circuit parameters, such as size of capacitors, length of pipeline, and oversampling ratio, among others; and (3) varying the bias currents of the opamps in proportion to the converter sampling frequency, accomplished through the use of a phase-locked loop (PLL). This converter also incorporates several power-reducing features such as thermal noise limited design, global converter chopping in the pipeline mode, opamp scaling, opamp sharing between consecutive stages in the pipeline mode, an opamp chopping technique in the delta–sigma mode, and other design techniques. The opamp chopping technique achieves faster closed-loop settling time and lower thermal noise than conventional design. At a converter power supply of 3.3 V, the converter achieves a bandwidth range of 0–10 MHz over a resolution range of 6–16 bits, and parameter reconfiguration time of twelve clock cycles. Its PLL lock range is measured at 20 kHz to 40 MHz. In the delta–sigma mode, it achieves a maximum signal-to-noise ratio of 94 dB and second and third harmonic distortions of 102 and 95 dB, respectively, at 10 MHz clock frequency, 9.4 kHz bandwidth, and 17.6 mW power. In the pipeline mode, it achieves a maximum DNL and INL of $\pm$0.55 LSBs and $\pm$0.82 LSBs, respectively, at 11 bits, at a clock frequency of 2.6 MHz and 1 MHz tone with 24.6 mW of power.**

***Index Terms*—ADC, analog-to-digital, chopping, delta–sigma, OSR, phase-locked loop, pipeline, PLL, programmable, reconfigurable, sigma–delta.**

I. Introduction

THERE ARE applications that require analog-to-digital converters (ADCs) that can digitize signals at a wide range of bandwidth at varying resolution with adaptive power consumption. One such application is a multistandard communications system. The trend toward an ever-increasing variety in communications applications, as well as the proliferation of standards for each of these applications, demands radio receivers that can be made to operate over a variety of specifications. A single converter that can be reconfigured to adapt to these various standards is highly desirable [1]. Yet another sought-after feature of a communication device is the possibility of adapting the performance of its electronics to its surrounding conditions [1]. Catering to such variable quality of service requires a digitization system that can adapt its power consumption with changing signal-to-noise and bandwidth specifications.

There are several popular ADC architectures, such as the flash, pipeline [2], cyclic [3], and delta–sigma converters [4]. Each of these architectures, however, can work optimally only at a narrow range of resolution, bandwidth, and power. For example, a standard pipeline converter works optimally at low-to-medium resolutions and medium-to-high speeds, while a delta–sigma converter works best at low speeds and delivers medium-to-high resolutions. A conventional ADC with fixed topology and parameters cannot efficiently be employed for the task of digitizing signals at a wide range of bandwidth at varying resolution with adaptive power consumption.

An alternate approach is to employ an array of ADCs, each customized to work at narrow ranges of resolution and input bandwidth. Such a converter implementation, however, would require a prohibitively large number of ADCs to achieve optimal power consumption with a reasonably fine granularity over input bandwidth and resolution.

A single ADC with reconfigurable parameters and reconfigurable topology would be able to achieve the above goal. Prior reconfigurable ADCs, however, achieve very limited reconfigurability. For example, variable resolution in a delta–sigma converter has been proposed by changing oversampling ratio (OSR) and bias currents of the converter over a predetermined set of values obtained from a lookup table [5]. This fixed arrangement can offer only relatively limited resolution reconfigurability. In addition, relying on predetermined bias currents does not work over different fabrication processes without costly calibration. Another ADC with limited configurability operates only at select values of 10-b/3-Msamples/s, 8-b/4-Msamples/s, and 4-b/8-Msamples/s [6]. Other examples of prior reconfigurable solutions include a flash ADC with two settings [7], [8] and a cyclic ADC that can be configured for 8, 13, or 16 bits [9]. Both of these provide only limited reconfigurability. This work proposes the idea of a single converter [10], [11] that can morph itself into different topologies to cover the desired continuum of resolution and bandwidth space with minimum power at each performance level. The proposed converter is designed to provide a significantly larger reconfigurability space.

II. Concept of Proposed Reconfigurable Converter

The concept of the proposed ADC stems from the observation that ADC architectures such as the pipeline, cyclic, and

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delta–sigma ADC topologies can cover a wide range of data rate and resolution. As mentioned in the previous section, while the pipeline is ideal for low-to-medium resolutions and medium-to-high speeds, the delta–sigma architecture can deliver very high resolutions at low-to-medium speeds. These ADC topologies, furthermore, are composed of the same basic components such as opamps, comparators, switches, and capacitors. The difference between them, from a network perspective, is the interconnection between these devices. Thus, a converter composed of these basic building blocks in conjunction with a configurable switch matrix can be made to construct these different topologies and work at different resolutions and bandwidths. At each point in the data rate versus resolution space, the ADC adjusts its topology to minimize the power consumption. Such a solution has one drawback: switch parasitics that lead to performance degradation. This problem has been addressed in the switch-capacitor sample/amplify/integrator core by maximizing the reuse of switches between different modes, as will be discussed in detail in a later section.

A. Reconfiguration Methodology

Reconfiguration of this data converter occurs at three levels.

1) Architecture reconfiguration. This involves the choice of either the pipeline or the delta–sigma topologies. The converter is in delta–sigma mode for resolution greater than 12 bits, while for lower resolutions, it is in pipeline mode.
2) Parameter reconfiguration. In the pipeline mode, the size of the capacitors and the length of the pipeline can be modified while the delta–sigma relies on variation of OSR to change its resolution. Variation of the OSR at a fixed input bandwidth as well as the variation of the input bandwidth in either of the modes demands a method by which the power consumption of the converter can track the sampling rate. This leads us to the third reconfiguration method.
3) Bandwidth reconfiguration. Here, a phase-locked loop (PLL) senses the clock frequency and varies the bias current of the opamps automatically to exactly the value that is necessary for the stage outputs to settle to the appropriate level at that clock frequency.

B. Selection of Architectural Modes

While the pipeline and cyclic converters contain similar components and are topologically similar, the cyclic converter has a lower figure-of-merit (FOM) than the pipeline converter employing scaled opamps [12], [13]. However, the cyclic converter is capable of digitizing at a lower sampling rate than the pipeline converter. The reason for this stems from the fact that the minimum clock speed of any converter is limited by leakage from the switched capacitors. For certain applications, nevertheless, the pipeline can be operated in burst mode or in oversampling mode to lower its effective sampling rate. Clearly, thus, the pipeline can do almost everything the cyclic can do, at lower power. This allowed us to eliminate the cyclic converter as a choice for one of the modes of the reconfigurable converter, resulting in reduced design complexity. Thus, only the delta–sigma and the pipeline architectures were eventually chosen as the primary modes of the reconfigurable converter.

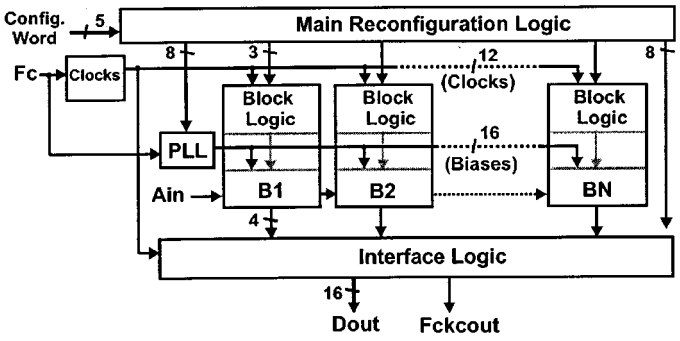


Fig. 1. ADC architecture.

III. ADC Architecture and Architecture Reconfiguration

A. System Level Description of Converter

The reconfigurable converter prototype shown in Fig. 1 contains a main reconfiguring logic that utilizes a user-defined *configuration word* to generate internal control bits to determine the global structure of the converter, the state of each of the basic building blocks B1–B8, and the other peripheral blocks of the converter as shown in the figure. The clock generator module uses the externally provided clock signal to create two nonoverlapping phases and two delayed versions of each phase. It then provides these six clock signals, along with their complements, to the block configuring logic of the cascaded basic building blocks and the other peripherals. In order to maximize signal range of the converter, the clock voltage is set to 4.6 V, which is higher than the analog power-supply voltage achieved by raising the power supply of the clock generator module. Normally, standard clock-boosting circuits, such as that described in [14], are used to boost up the clock level. For simplicity, clock-boosting circuitry was not included in this prototype. The PLL utilizes the clock, and determines the appropriate bias current of the converter based on the clock frequency and the resolution desired of the converter. The output interface consists of several registers for the task of temporal and spatial alignment of the output digital bits. The output interface then feeds the processed data to the output drivers that send the information out of the chip. The basic building block of the converter (represented by B1–BN in Fig. 1) is described in greater detail in Section VI.

B. Pipeline Mode Architecture

In the pipeline mode, the switched-capacitor portion of each block is transformed to a sample-and-hold and multiply-by-2 stage for two consecutive pipeline stages, as will be explained later. The pipeline mode also incorporates a 1.5-b/stage digital error correction scheme [15] that digitally compensates for the offset of the comparator. This implementation of this technique requires two comparators with thresholds at $\pm V_A$, where $0 < V_A < V_{\mathrm{REF}}/2$. Ideally, V_A equals $V_{\mathrm{REF}}/4$. This comparator pair is contained within the decision block shown in the illustration of the basic building block. The consequence of using the digital error correction is that offset from the opamp (as long as it is less than $V_{\mathrm{REF}}/2$) no longer saturates the next stage of the pipeline ADC. Thus, the offset of each opamp can be simply modeled as a shift in the residue plot of the pipeline

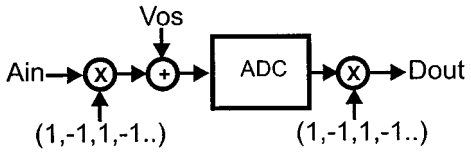
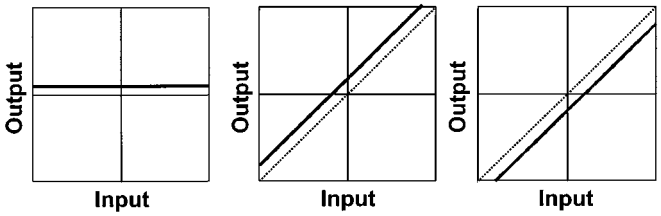


Fig. 2. Illustration of global chopping of ADC.

stage, implying that these opamp offsets can be referred to the input of the converter as a single global offset. To cancel this global converter offset, a global converter chopping mechanism is proposed, as is described below. In contrast to the proposed chopping, conventional offset cancellation either requires the opamp to be active during the sampling phase or involves additional circuitry, leading to greater power and complexity.

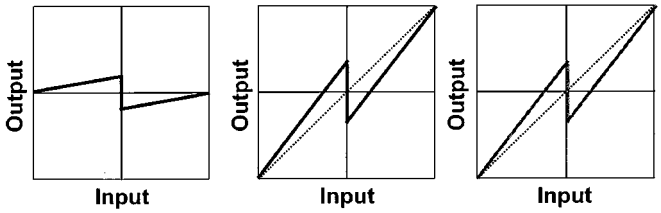
The proposed global converter-chopping scheme entails multiplying the input of the converter by a string of alternating 1's and -1's, as shown in Fig. 2, thus modulating the converter input to a higher frequency away from the dc offset and $1/f$ noise of the converter. The output is multiplied by an identical string to demodulate the input signal back to the baseband. The offset and $1/f$ noise are consequently displaced to $F_S/2$ and subsequently removed by low-pass digital filtering. Input chopping is achieved simply by swapping the positive and negative inputs every clock cycle, while output chopping is achieved by inverting the sign of the digital output every other clock cycle. Global chopping of the ADC eliminates errors with even symmetry in the ADC transfer characteristic, while leaving errors with odd symmetry undisturbed. To understand this, refer to Figs. 3 and 4. Fig. 3 shows the case for ADC with errors having even symmetry. Fig. 3(a) shows the error, while Fig. 3(b) and (c) shows the transfer characteristic with the even error superimposed on it for the unchopped sample and for the chopped sample, respectively. It is clear that averaging the characteristics (through the process of digital filtering) in Fig. 3(b) and (c) will lead to the ideally desired characteristic. Fig. 4(a), (b) and (c) shows the corresponding plots for odd symmetry error. Averaging the characteristics in Fig. 4(b) and (c) will not remove the error. As far as the impact of global chopping on linearity, ADC characteristics containing integral nonlinearity (INL) and differential nonlinearity (DNL) can contain both even and odd symmetric components. Global chopping only serves to remove the symmetric portion of these errors.

Global offset compensation is not only simpler to implement than local opamp offset correction schemes, it can also address offset due to other sources, such as charge injection from switches in the switched-capacitor circuit. Again, it has to be ensured that the internal opamp offsets do not saturate the following stages. Practically, this is done by the use of the 1.5-b/stage digital error correction scheme. Since opamp offset cancellation is not performed at a local level, the global chopping scheme frees up the opamp during the sampling phase. As a result, consecutive stages of the pipeline do not both simultaneously require the opamp, and a single opamp can be timeshared [13], [16] between the two consecutive stages, leading to power and area savings. This allows two stages of the pipeline architecture to be collapsed into one basic building block containing a single opamp and several capacitors.



(a) (b) (c)

Fig. 3. Effect of global chopping on ADC transfer characteristic with even symmetry. (a) Error of ADC transfer characteristic. Error has even symmetry. (b) ADC transfer characteristic with even symmetry error for unchopped sample. (c) ADC transfer characteristic with even symmetry error for ADC in chopped condition. Averaging the transfer characteristics shown in (b) and (c) will yield the ideal ADC transfer characteristic. The characteristic in (c) has been obtained by flipping the input and output axes of the characteristic shown in (b).



(a) (b) (c)

Fig. 4. Effect of global chopping on ADC transfer characteristic with odd symmetry. (a) Error of ADC transfer characteristic. Error has odd symmetry. (b) ADC transfer characteristic with odd symmetry error for unchopped sample. (c) ADC transfer characteristic with odd error for ADC in chopped condition. Averaging the transfer characteristics shown in (b) and (c) will not change the error.

Since successive stages of the pipeline architecture contribute less noise, the pipeline stages can employ capacitors and opamp sizes and power that are successively scaled. Theoretical MATLAB analysis shows that the optimal interstage scale factor is in the range of 0.4 to 0.6. Most importantly, however, it is found that this optimal scale factor is quite broad. The fact that the minima is broad allows us to choose a convenient factor of 0.5 as the interstage scale factor; since two pipeline stages are contained within one block of the reconfigurable ADC, the interblock scaling factor is 1/4. The choice of 0.5, as we will see, paves the way for a novel parameter reconfiguration methodology when the converter is in the pipeline mode.

C. Delta–Sigma Mode Architecture

The delta–sigma mode of the reconfigurable ADC is based on a fourth-order distributed feedback/distributed feedforward cascade-of-integrators-type architecture [17], as shown in Fig. 5. These four delta–sigma stages are embedded in the first four reconfigurable converter blocks, with each basic building block corresponding to a single delta–sigma stage. Global ADC chopping cannot be employed with a low-pass delta–sigma converter to eliminate opamp offset and $1/f$ noise. This is because the process of chopping the input modulates the input band to $F_S/2$. Opamp offset in the delta–sigma mode is corrected by executing opamp chopping in the first block. Its circuit implementation is described in Section VI-C. In the delta–sigma mode as well, the opamps in the successive stages can be scaled by a factor dependent on the oversampling ratio. While the interblock scale factor of 1/4 is less than the optimal

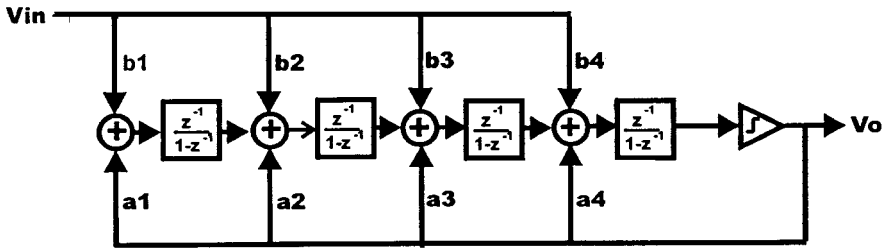


Fig. 5. Architecture of converter in delta–sigma mode.

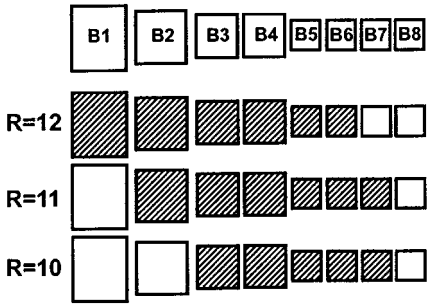


Fig. 6. Resolution variation in pipeline mode.

scaling factor for the range of oversampling ratios employed, it is enough to extract most of the power savings stemming from the process of scaling.

IV. ADC Parameter Reconfiguration

With the chosen interstage scale factor of 1/2, the thermal noise from the second block in the reconfigurable converter B2 is twice as high as that from B1, as shown in Fig. 1. This leads to the resolution reconfiguring methodology in the pipeline ADC as illustrated in Fig. 6. A 12-b mode pipeline employs blocks B1–B6. An 11-b mode pipeline can tolerate twice as much thermal noise and employs blocks B2–B7, the 10-b mode employs blocks B3–B7, and so on. Any block that is not used is switched off. Thus a combination of shifting and truncating maintains kT/C-limited operation and hence minimum power through varying resolution. This process requires the input to be physically routed to several stages of the pipeline; this, however, is necessary in any case because the delta–sigma architecture involves distributed feedforward of the input.

In the delta–sigma mode, resolution is varied by changing the oversampling ratio of the converter. The thermal noise contributing capacitors in delta–sigma mode are reused from the pipeline mode. For this reason, the delta–sigma mode is in thermal noise dominated regime for most oversampling ratios. In this regime, varying coefficients of the modulator to change the resolution is not very efficient.

V. Bandwidth Reconfiguration

Bandwidth reconfiguration is achieved using a PLL. Fig. 7 shows the PLL employed for this purpose. The voltage-controlled oscillator (VCO) shown to the right of the figure is constructed from three amplifiers that are scaled-down replicas of the opamps of the ADC in such a way that the VCO frequency F_{VCO} is proportional to the unity-gain frequency of these opamps, which in turn corresponds to the settling speed of the opamps in the ADC. The output of the charge pump is converted to a current and is then used as the bias current of the VCO opamps to control its oscillation frequency. The same bias current is also fed to the opamps in the main ADC. The ADC sampling clock is supplied to the input of the PLL. During locked conditions, the bias current of the VCO is exactly such that the VCO oscillation frequency matches the sampling clock frequency. This automatically fixes the bias currents of the ADC opamps. If the clock frequency changes, the ADC bias current changes so that the settling time of the ADC remains synchronized to the clock frequency. In practice, the settling time of the ADC also depends on the resolution of the ADC. Higher resolution requires finer settling and hence more settling time. This is taken care of by increasing the capacitive load of the VCO opamps as resolution increases. For the same clock frequency, greater VCO capacitance causes larger bias currents to flow through the opamps. A set of switchable capacitors is placed at the output of each VCO opamp to accomplish the capacitive load variation.

VI. ADC Basic Building Block Circuits

A. Block Diagram of Basic Building Block

The internal structure of each basic building block is shown in Fig. 8. It possesses the capability to serve as sample-and-hold and gain stages for two consecutive stages of the pipeline architecture in the pipeline mode and as a multiple input integrating summer while in the delta–sigma mode. Each building block consists of a block reconfiguration logic, an opamp, several capacitors and switches, a programmable decision box, and an output conditioning logic. The block reconfiguration logic obtains the reconfiguration information from the main reconfiguration logic and creates several static signals for the various parts of the block. Based on the control information it receives from the main reconfiguration logic, it also conditions the clocks that the block receives from the main clock generator. Clock conditioning entails controlling the status of the clocks (active or inactive), determining which phase and delayed version of the clock is fed to switches of the switch-capacitor network. The output-conditioning block determines the flow of the data from each of the blocks to the output interface of the ADC and its neighboring blocks. In particular, it determines which of the bits to allow outside of the block depending on a variety of control signals.

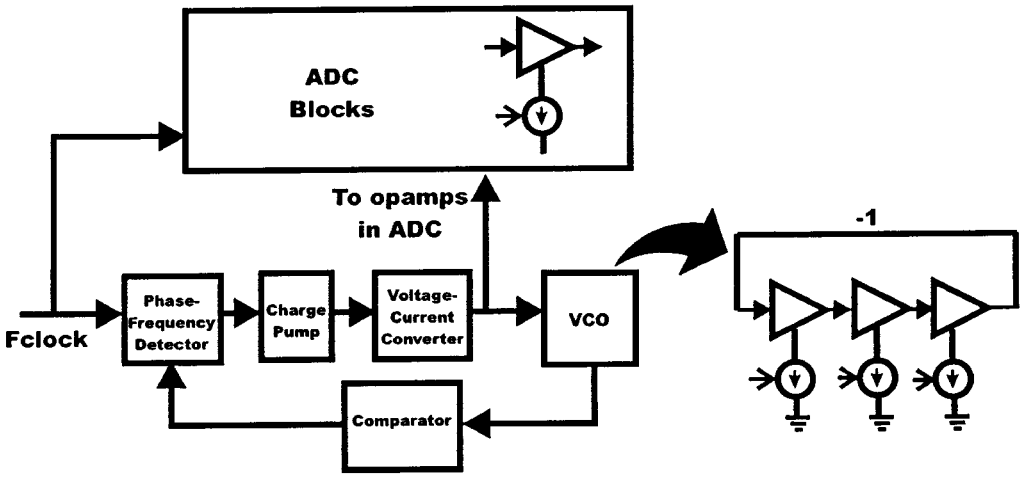


Fig. 7. Bandwidth reconfiguration with a PLL.

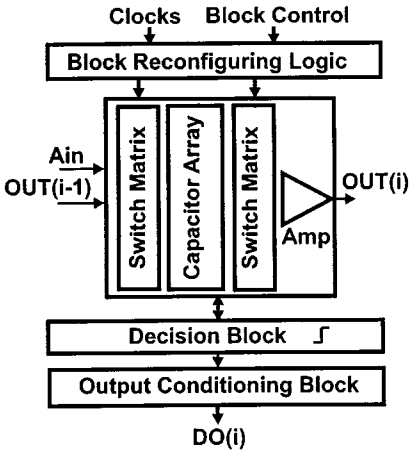


Fig. 8. Structure of basic building block.

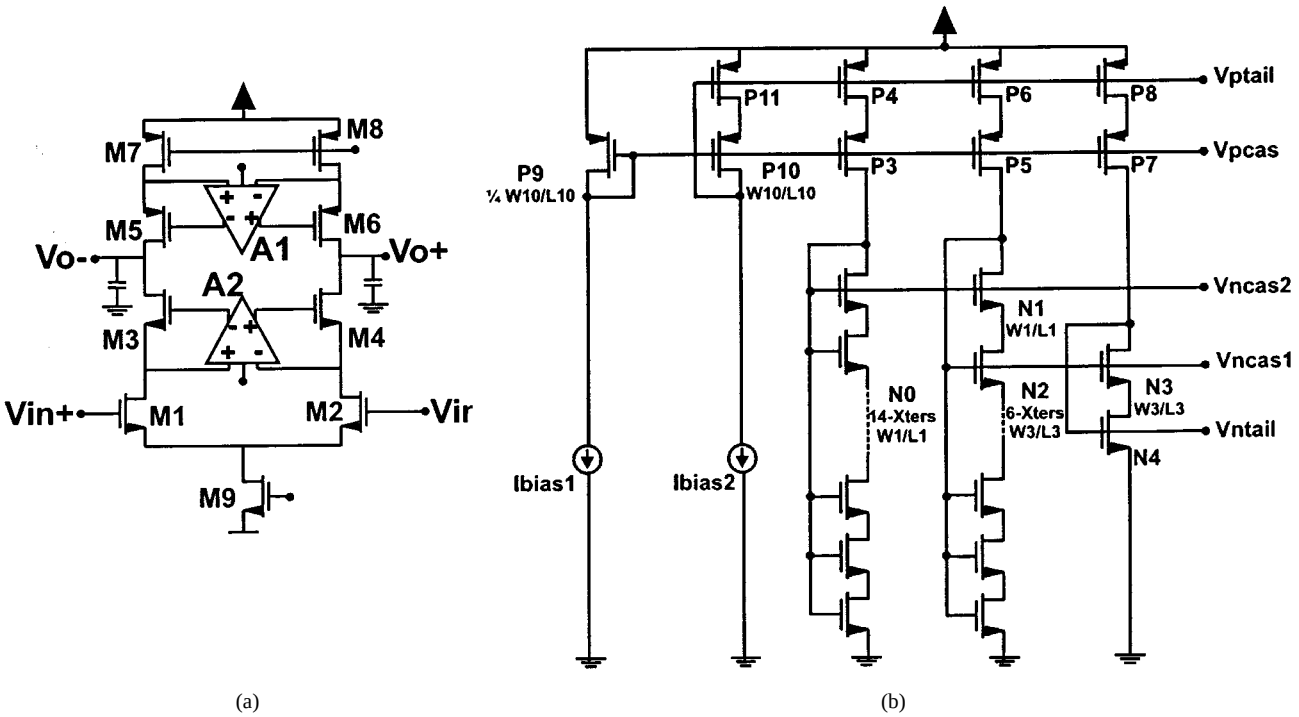
B. Operational Amplifier

A gain-enhanced telescopic architecture, shown in Fig. 9(a) was used as the basic opamp structure because of its high speed and low power. A standard switched-capacitor circuit is employed for the common-mode feedback with its feedback node at the gate of the pMOS load transistors. The gain enhancement amplifiers [18] use a standard folded-cascode architecture; the choice of architecture was determined by requirements of speed and desired input/output voltage levels. Since the gain enhancement amplifiers drive much smaller capacitive loads than the main amplifier, it is possible to scale down these circuits with respect to the main amplifier. After scaling, the power consumed by both gain-enhancement amplifiers combined is about a third of the total power consumption of the opamp.

The bias circuit employs the well-known high-swing current mirror [19]. As much as possible, the bias circuits for the main topology and the gain-enhancement amplifiers are shared. Fig. 9(b) shows the bias circuit for the opamp in the first block. To implement transistors N0 and N2 with an effectively smaller width, transistors were placed in series. The bias circuit has been designed in order to keep all the opamp transistors in saturation in the strong-inversion or subthreshold regimes as the bias current is varied. In the strong-inversion regime, the transistors are sized such that the tail transistor M9 in Fig. 9(a) has $\Delta V + V_{\rm MAR} + \Delta V_{\rm T}$ across its drain–source terminals, where ΔV corresponds to $V_{\rm GS} - V_{\rm T}$ of a MOSFET, $V_{\rm MAR}$ is a margin voltage that designed to be a certain fraction of ΔV, and $\Delta V_{\rm T}$ corresponds to $V_{\rm T,N2} - V_{\rm T,M1}$. Here $V_{\rm T,N2}$ is the effective threshold voltage of the series transistors that N2 is comprised of and $V_{\rm T,M1}$ is the threshold voltage of the input transistors of the opamp in Fig. 9(a). The body terminal of each series transistor in N2 is deliberately tied to ground to make $\Delta V_{\rm T,N2} > \Delta V_{\rm T,M1}$. As bias current is reduced and all the transistors move into the subthreshold regime, ΔV and $V_{\rm MAR}$ (which is a function of ΔV) go to zero, however, $\Delta V_{\rm T}$ is still available across the drain-to-source terminals of tail transistor M9 to maintain it in saturation. $\Delta V_{\rm T}$ is approximately 3 kT/q or about 75 mV, which is adequate to keep the tail in saturation in the subthreshold regime [20]. Through these two regimes, it is important to ensure that the current from the PLL is appropriate to what the opamps desire. By way of design, the oscillation frequency of the VCO is directly related to the unity-gain frequency of the opamps, implying that the bias current provided by the PLL is linearly proportional to the clock frequency. In the subthreshold regime, both the small-signal settling speed and the slewing speed of the opamps vary linearly with bias current. In the strong-inversion regime, while the slewing speed continues to vary linearly with current, the small-signal settling speed varies as the square root of the current. If the current from the PLL and the optimal current for the ADC opamps is matched at the transition point when the transistors move from subthreshold to the strong-inversion regimes, the PLL will supply the optimal current throughout the subthreshold operation. However, as the transistors go into the strong inversion, the PLL gradually supplies more than optimal current to the opamps. This difference is insignificant for maximum clock frequency of 20 MHz for this design.

C. Switched-Capacitor Network

Fig. 10(a) shows a typical switched-capacitor half network for a typical block in the converter. It employs six capacitors and several input and output switches. Fig. 10(b) shows the signal paths that are active when the system is in the pipeline



(a) (b)

Fig. 9. (a) Opamp used in blocks B1–B5. The opamps in blocks B6–B8 are topologically identical without the gain enhancement amplifiers. (b) Typical bias circuit employed for the amplifiers.

mode. In this mode, the capacitors Cf and Cc, at the top of the figure, along with their corresponding switches, are deactivated. The capacitors C1 and C2, at the bottom, are employed for implementing the first stage of the block in the pipeline mode, while capacitors C3 and C4, in the middle, are employed in the second stage of the block in this mode. The value of C1 and C2 in block B1 is 400 fF, while capacitors C3 and C4 are sized down to 200 fF in keeping with an interstage scale factor of 1/2. Fig. 10(c) shows the switched-capacitor circuit when the converter is in delta–sigma mode. In this case, the capacitor pair in the middle comprising C3 and C4 are switched off. Capacitors C1, C2, and Cc are used to implement the coefficients b, a, and c, as shown in Fig. 10(d), respectively. Cf is wrapped around the opamp to serve as the feedback capacitor. The load of the opamp in the two phases is equalized by sizing the common-mode feedback fixed and refreshing capacitors appropriately. This ADC has 44% extra switch parasitic capacitance at the opamp inputs compared to a conventional pipeline converter. However, considering the interconnect capacitance at the opamp inputs as well, this overhead is lower. The exact numbers, of course, depends on the implementation and switch sizes. For the reconfigurable converter implemented here, the interconnect capacitance is quite large. Taking interconnect capacitance into account, for the first stage in the first block of the pipeline mode, the overall parasitic capacitance at the inputs of the opamp increases by approximately 24%.

To minimize the effect of offset and $1/f$ noise on the performance of the converter in the delta–sigma mode, the first block opamp is chopped at half the sampling frequency. A conventional implementation of opamp chopping is depicted in Fig. 11(a). Switches are employed in series with the input and output of the opamp to chop the opamp at $f_s/2$ frequency without regard to the rest of the switched-capacitor circuit. These switches introduce higher order poles to the closed-loop opamp system, leading to slower overall converter speed. In the proposed implementation [21], shown in Fig. 11(b), instead of chopping the opamp, the charge packet that is delivered to the opamp and its integrating capacitor is chopped between the positive and negative inputs of the opamp. In one clock period, the charge from $V_{\rm in}+$ is fed to the positive terminal of the opamp, while in the next the charge from $V_{\rm in}+$ is delivered to the negative terminal. In order to maintain the same transfer function, capacitor Cf+ and Cf− also are interchanged every other clock period, while the next stage samples the $V_{\rm o}+$ and $V_{\rm o}-$ terminals alternatively every clock period. In other words, the charge packets are chopped around the opamp. This operation leads to the same effect as conventional opamp chopping. This chopping mechanism eliminates the switches from inside the closed loop feedback around the opamp. Although these parallel switches still contribute some parasitic capacitance, an analysis shows that the total parasitic capacitance at the opamp inputs is also reduced to about 4/7 of its original value. Note that the switches next to integrating capacitors Cf+ and Cf− are needed in both cases for the purposes of resetting the system in case of modulator instability. Removing the switch resistance in series with the opamp inputs and outputs leads to faster settling time and/or lower power compared to the conventional chopping mechanism. Additionally, the thermal noise level of the proposed configuration is also lower compared to the conventional approach, because there is no switch resistance in series with the opamp input within the loop. This scheme also allows the implementation of offset chopping in the delta–sigma mode without reducing the performance level of the converter in the pipeline mode.

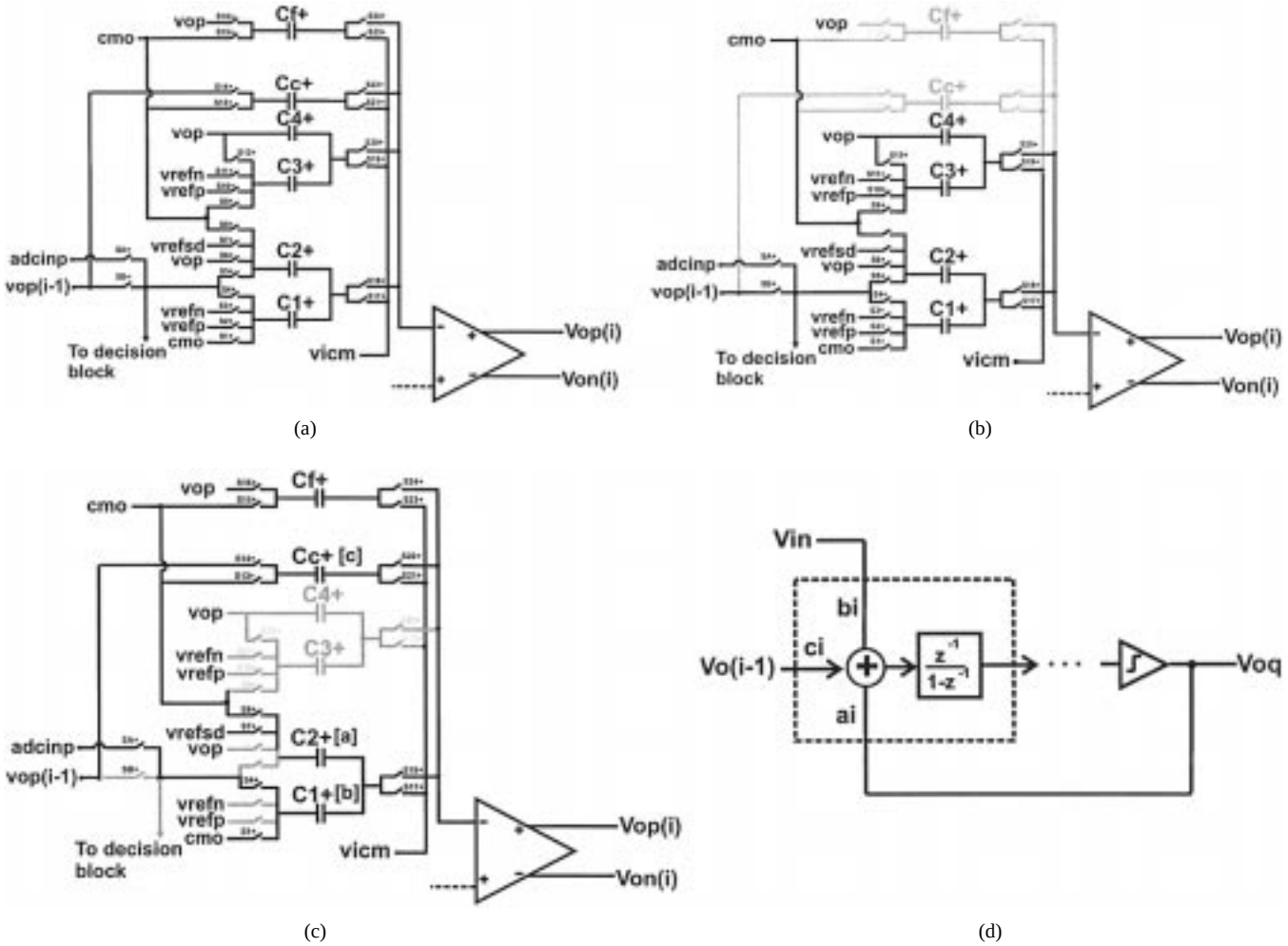


Fig. 10. Switched-capacitor core in basic building block. (a) All switches shown. (b) Switched-capacitor core in pipeline mode. (c) Switched-capacitor core in delta–sigma mode. (d) Simplified structure of block in delta–sigma mode.

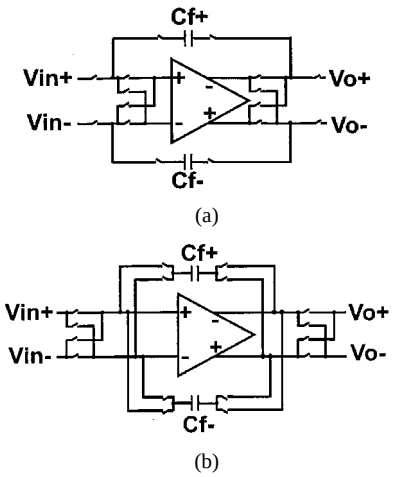


Fig. 11. Illustration of opamp chopping to minimize opamp offset and $1/f$ noise. (a) Conventional opamp chopping scheme. (b) Proposed opamp-chopping mechanism.

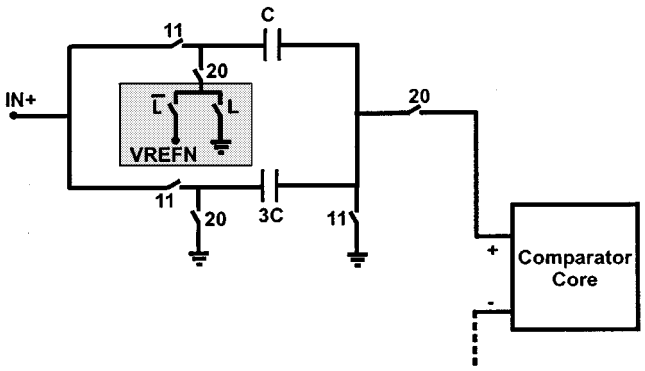


Fig. 12. Switched-capacitor circuit details of each comparator.

D. Decision Block

Different blocks in the reconfigurable converter require their comparators to have different thresholds at different times. For example, in the pipeline mode, all blocks except for the last require comparator thresholds of $\pm V_{\rm ref}/4$ in both its stages; on the other hand, the last block in the converter requires zero thresholds from its comparator in the second stage. In the delta–sigma mode, the last block requires zero threshold from its comparators, while the other comparators can be disabled. Due to these variable requirements, a programmable comparator, shown in Fig. 12, was created. It consists of a switched-capacitor circuit followed by a latch. If the block containing the comparator is the last active block, the variable L, as shown in the figure, is high; consequently, the switched-capacitor circuit shifts the sampled voltage signal IN+ (or IN−) by $V_{\rm REFN}/4$

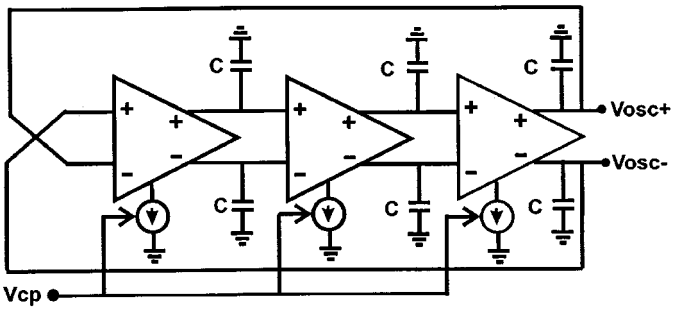


Fig. 13. VCO construction.

(or $V_{\mathrm{REFP}}/4$) before presenting the signal to the latch. Simple analysis shows that this condition will implement a comparator threshold of $V_{\mathrm{REF}}/4$. If the block is not the last active block, on the other hand, the sampled input IN+ (or IN−) is presented to the latch inputs without a shift, effectively implementing a zero comparator threshold. Hence, based on whether the L bit in the figure is 1 or 0, the comparator either implements zero threshold or a $\pm V_{\mathrm{REF}}/4$ threshold. There are a total of four such comparators, a pair for each stage within the block.

VII. PLL Design

The opamp employed in the VCO has a standard telescopic architecture without the gain-enhancement amplifiers and is an exact replica of the smallest telescopic amplifier used in the converter, the amplifier employed in blocks B3–B8. To construct the VCO, three opamps are cascaded together, differentially, in a loop, as has been described earlier and shown in Fig. 13. For simplicity, every opamp has its own bias circuit. Diode limiters are placed at the output of opamps to restrict the swing of the oscillator opamps to about 600 mV, which is about 1/4 of the overall swing of the opamp. They reduce the dependence of the oscillation frequency on slewing time, making the VCO oscillation frequency depend more on the small-signal characteristics of the VCO opamps.

The post-VCO comparator converts the sinusoidal signal from the VCO to digital levels. An open-loop telescopic opamp that is a replica of the VCO and ADC opamp is employed as the comparator. The bias current through this comparator opamp is varied exactly in same manner as the VCO opamps. This implies that the unity-gain frequency of the comparator opamp tracks the unity-gain frequency of the VCO opamps. Since the input to the comparator is a sinusoidal waveform that is proportional to these unity-gain frequencies, the gain of the comparator opamp will remain constant regardless of the clock frequency. The common-mode level of the sinusoidal waveform from the VCO is set to track the optimal input common-mode level of each of the telescopic opamps of the VCO. As the bias current varies in response to the changing clock frequency, this common-mode level will also change. Since the comparator opamp is a replica of the VCO opamps and its current is set to always equal the current in the VCO opamps, the optimal input common-mode level of the comparator is always equal to the common-mode level of the sinusoidal input ensuring that the common-mode level of the VCO oscillations exactly corresponds to the common-mode level required by the comparator.

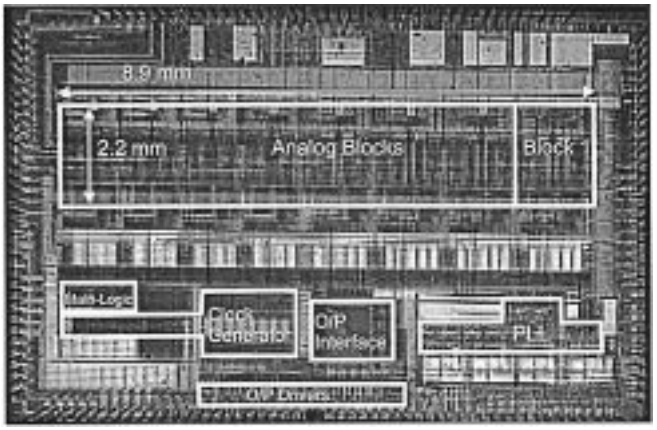


Fig. 14. Proof-of-concept prototype of reconfigurable converter. The layout is optimized for maximum testability of chip.

The charge pump for the PLL has been implemented in such a way as to minimize the charge sharing between the internal charge-pump nodes and the charge-pump load capacitor. The passive loop filter elements employed at the output of the charge pump is placed off chip. A single transistor is employed to convert the voltage applied at its gate to a current that varies over four orders of magnitude over the operating range of the converter. The voltage at the gate of this transistor is filtered using an off-chip *RC* filter and then used to synthesize an array of weighted currents for the opamps in the ADC.

VIII. Experimental Results

The reconfigurable converter was built in a 0.6-μm CMOS process. Its operation has been validated over a bandwidth of 1 Hz to 10 MHz and resolution ranging from 6 to 16 bits. Fig. 14 illustrates a prototype used as a proof-of-concept vehicle for the reconfigurable converter. While the overall area is large, it arises from nonoptimal layout, as well as large chunks of the chip devoted for maximizing flexible testing of the converter. A conservative estimate of active area for the chip is 5.5 mm^2, and this area is also expected to shrink in an optimally designed reconfigurable layout. A detailed analysis of the layout and circuit suggests that an optimal layout of the reconfigurable converter would occupy approximately 20%–30% over and above a single pipeline converter designed for 12 bits of resolution and operate at the highest frequency that can be expected from this design.

Fig. 15(a) and (b) shows the measured fast Fourier transform (FFT) of the converter output for a sample performance point of the reconfigurable converter. The x-axis in Fig. 15(a) ranges from 0 to 0.5 fs. In this case, at a clock frequency of 10 MHz and an OSR of 512, the converter possesses a signal-to-noise ratio (SNR) of 93.9 dB. The second and third harmonics are 102.4 and 95 dB, respectively, below the signal. Fig. 15(c) shows the relationship between the analog power consumption and the SNR of the converter at varying OSR. Here, the input tone is held constant at 6.25 kHz and the clock frequency is varied. It is evident from this plot that there is a tradeoff between power and SNR. It is this tradeoff that the reconfigurable converter exploits. Fig. 15(d) shows the SNR as the input bandwidth is increased at a fixed clock frequency. Since the clock frequency is fixed, the power consumption is also fixed. Hence,

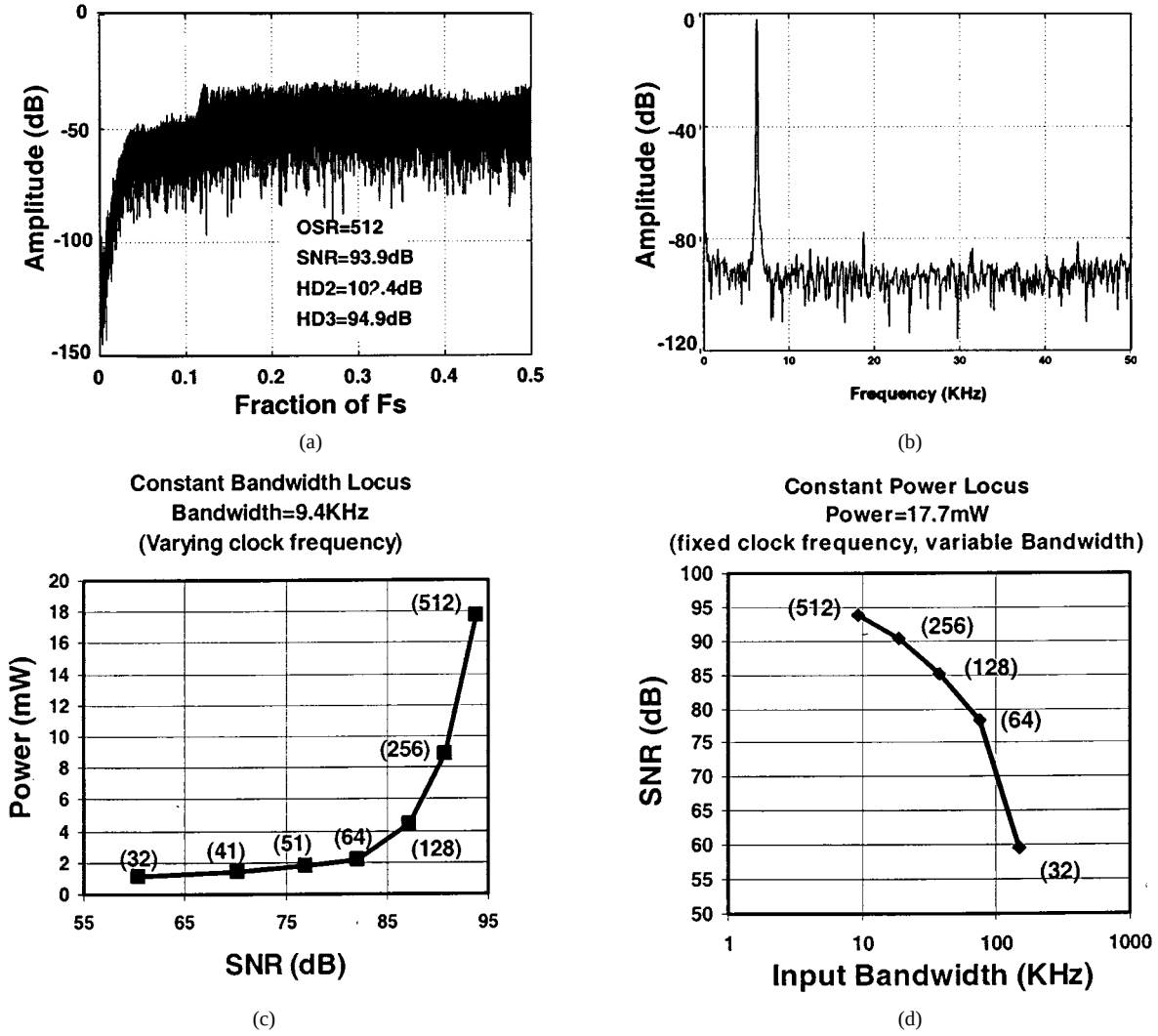


Fig. 15. (a) Converter output sample performance point in delta–sigma mode. (b) Converter output sample performance point in delta–sigma mode. (c) Measured variation of analog power with varying SNR for changing oversampling ratio (shown in parenthesis). (d) Variation of SNR with input bandwidth at fixed clock frequency. The oversampling ratio at each point is shown in parenthesis.

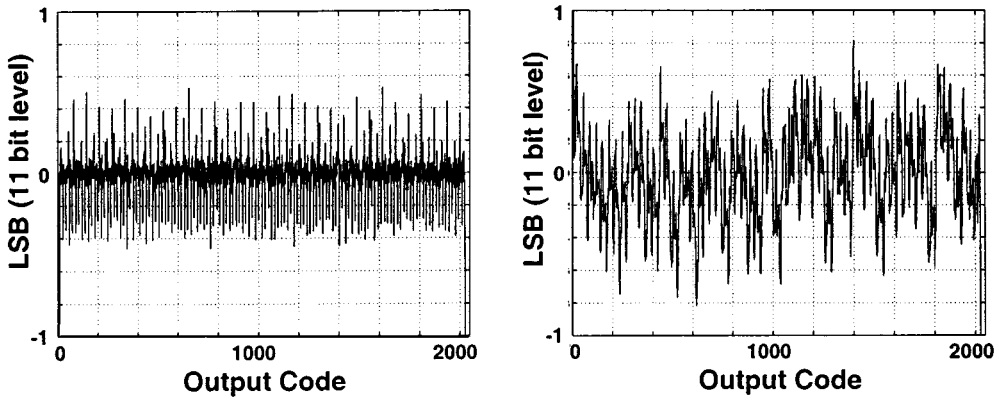


Fig. 16. (a) Differential nonlinearity. (b) Integral nonlinearity.

the curve shown is a constant power locus. Activation of the first block opamp chopping reduces the dc offset component by about 16–18 dB, respectively, and improves the SNR by 1 dB (at an OSR of 512). Larger SNR improvements are possible at higher OSR levels.

Fig. 16(a) and (b) shows the DNL and INL, respectively, of the converter in the 11-b pipeline mode. At 12 bits, the measured INL and DNL exceeded ± 1 LSB due to mismatch among the small capacitors that we used. Standard digital calibration [22], which for simplicity was not implemented on this chip,

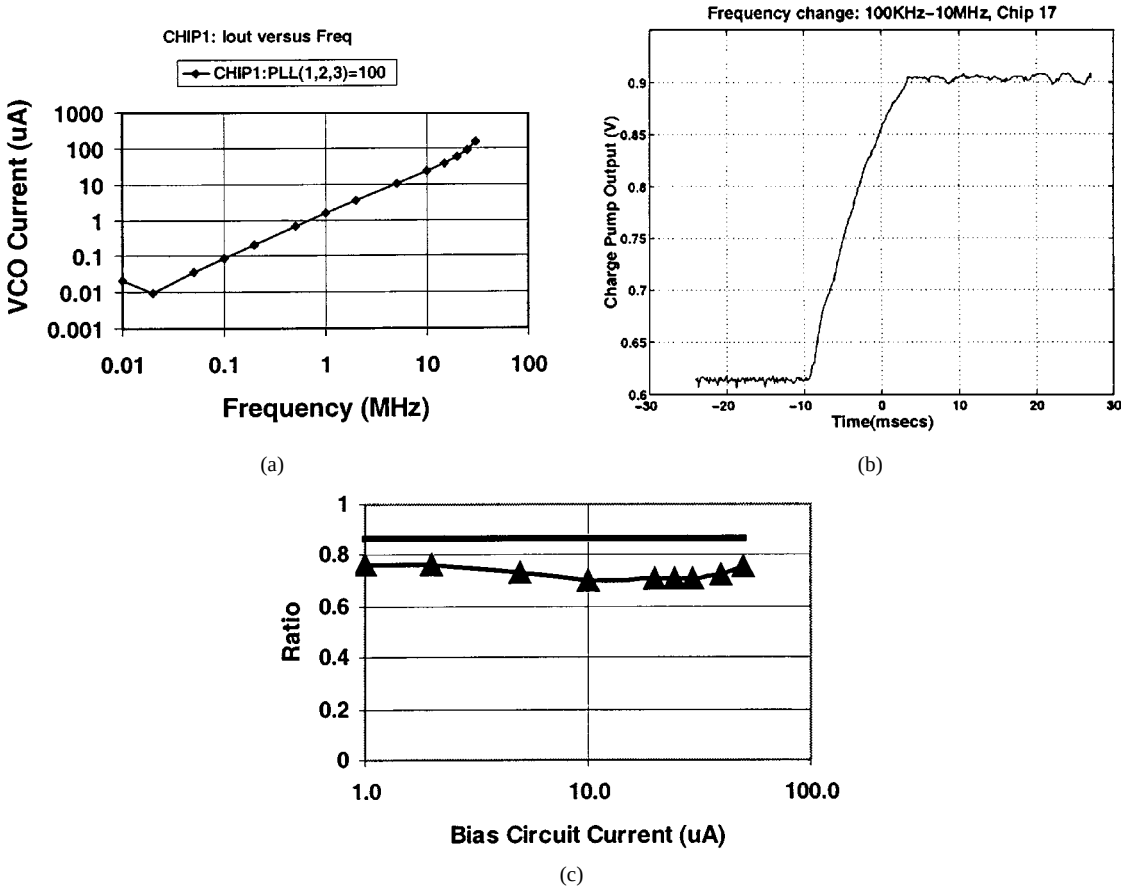


Fig. 17. (a) Variation of opamp bias current with varying clock frequency. (b) PLL dynamics for $C_{\rm cp} = 470$ nF and $I_{\rm cp} = 10\ \mu$A. (c) Simulated relationship between the VCO oscillation frequency and unity-gain frequency. The horizontal line shows the theoretical prediction of the ratio between the VCO oscillation frequency and the unity-gain frequency.

would correct this problem. Global offset correction reduces the dc offset by 32.5 dB.

Fig. 17(a) illustrates the tracking range of the PLL. The VCO opamp bias currents track the clock frequency over three orders of magnitude while it is varied between 20 kHz and 40 MHz. Fig. 17(b) shows the settling behavior of the PLL when the clock is varied from 100 kHz to 10 MHz. The settling time is 14 ms for an off-chip charge pump capacitive load and current of 470 nF and 10 μA, respectively. The slewing time expected for the PLL based on design values and the voltage shift in the measurement is 14 ms. This agrees very well with obtained measurements. Some noise is visible on the measured waveform that is partially due to measurement noise and partially due to high-frequency voltage noise due to the charge pump and the phase-frequency detector. The operation of the PLL is based on the premise that the VCO oscillation frequency is a constant factor times the unity-gain frequency of the opamps used in the VCO. Fig. 17(c) is included from HSPICE simulations to demonstrate that this is indeed true for a wide range of bias current variation.

In Fig. 18, the performance of the reconfigurable converter is compared to the measured performance of several custom converters published in the *IEEE International Solid-State Circuits Conference Digest of Technical Papers* and the IEEE JOURNAL OF SOLID-STATE CIRCUITS over the past three years. For completeness, converters fabricated with a variety of feature lengths and power supplies have been considered. The smallest feature

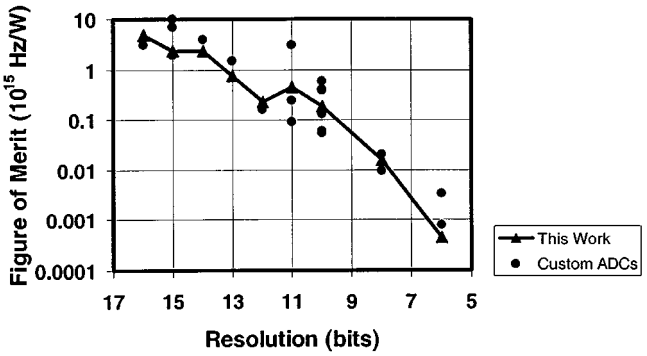


Fig. 18. Comparison of FOM of reconfigurable converter to custom-built converters published in the *IEEE International Solid-State Circuits Conference Digest of Technical Papers* and the JOURNAL OF SOLID-STATE CIRCUITS from 1997 to 2000.

length considered is 0.18 μm, while the highest supply voltage considered is 5 V. The converters considered include those that are distinguished by their performance in terms of speed as well as in power consumption. The definition of the FOM considered for this comparison is

$$\text{FOM} = \frac{2^{2N} \times (\text{Data Rate})}{\text{Power}} \tag{1}$$

where N, Power, and Data Rate refer to the resolution, power consumption, and output data rate of the converter, respectively.

TABLE I
PERFORMANCE SUMMARY OF RECONFIGURABLE CONVERTER

Process		**0.6μm CMOS, DPTM**	
Total Die Area (including pads) **Total Active Area**		**10.5mm x 7.6mm** **5.5mm^2**	
Power Supply		**2.7V-4.6V, 4.6V**	
Architecture and Parameter Reconfiguring Time		**12 clock cycles**	
Bandwidth Reconfiguration Time		**14ms (with Ccp=470nF)**	
PLL Lock Range		**20KHz-40MHz (with Ccp=470nF)**	
Delta-Sigma 16-bit Mode (3.3V)		**Pipeline 12-bit Design Mode (3.3V)**	
Resolution	**16 bits**	**Resolution**	**11 bits**
Fclock	**10MHz**	**Fclock**	**2.62MHz**
Fin	**6.25KHz (1.5V p-p diff.)**	**Fin**	**1MHz (1V p-p diff.)**
OSR	**512**	**Power**	**24.6mW**
Power	**17.7mW**	**DNL**	**< +/- 0.55LSB**
SNR	**94.4dB**	**INL**	**< +/- 0.82LSB**
HD2	**102dB**		
HD3	**95dB**		

Notice that the average FOM for all of the converters represented in the figure drop with reducing resolution. The primary chip statistics and two specific performance points of the converter are summarized in Table I. The architecture and parameter reconfiguration time is twelve clock cycles regardless of the clock frequency. This is because this time is primarily limited by the speed of the discrete-time switched-capacitor common-mode feedback circuit across the opamps.

IX. CONCLUSION

A reconfigurable ADC that can digitize signals over a bandwidth range of 0–10 MHz and a resolution range of 6–16 bits with adaptive power consumption has been proposed and described. It accomplishes its wide reconfiguration range through three levels of reconfiguration. The first level is architecture reconfiguration where the converter can be placed in either the delta–sigma or the pipeline modes. The second level is parameter reconfiguration, where a variety of variables such as capacitor values and converter length in the pipeline mode and oversampling ratio in the delta–sigma mode can be varied to tune the SNR. Finally, the bandwidth of the converter opamps can be tuned using a PLL scheme.

This paper also proposes global offset chopping to eliminate opamp offset in the pipeline mode. This scheme requires no additional power, is simple, and can also address offset from charge injection and other sources. In the delta–sigma mode, a new switched-capacitor implementation of opamp chopping is proposed. This technique requires no switches in series with the opamp inputs and outputs and thus can lead to faster closed-loop settling and lower thermal noise compared to its conventional counterpart. The PLL employed uses a VCO constructed using a cascade of opamps that are replicas of the converter opamps. This PLL method allows the opamp bias currents to be varied continuously over the continuum of data rate and works over almost four orders of bias-current variation. The switched-capacitor core in the converter has been designed in order to minimize the capacitive load overhead in each of the two architectural modes. The bias circuit has been designed in order to keep all opamp transistors in saturation in both strong-inversion and subthreshold regimes.

As a result of the above features, as well as other circuit designs described in the paper, the converter demonstrates measured performance that is comparable with state-of-the-art custom-built converters over a wide range of operating conditions.

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