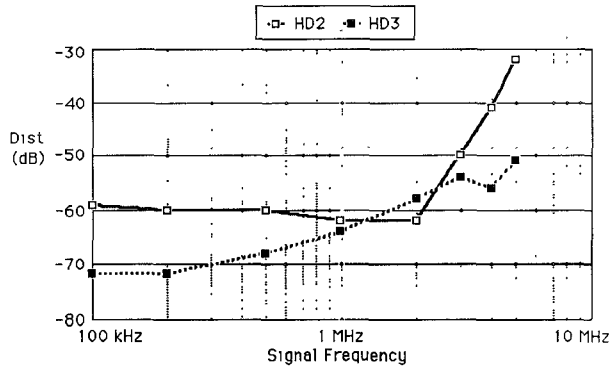


Fig. 3. Measured second and third harmonic distortion components of buffer as a function of frequency, for a ±1-V peak-to-peak sinusoidal input signal

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# The Effects of Oxide Traps on the Large-Signal Transient Response of Analog MOS Circuits

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*Abstract* — **Hysteresis in the threshold voltage of MOSFET's due to oxide traps can impose serious limitations on the accuracy and speed of analog circuits. The measured magnitude of the input-referred hysteresis ranges from 100 μV to more than 1 mV in NMOS devices stressed with positive gate–source voltages ranging from 1 to 5 V on microsecond-to-millisecond time scales. This hysteresis is explained by a model in which electrons tunnel to oxide traps close to the interface.**

## I. Introduction

Hysteresis in the threshold voltage of MOSFET's can limit the accuracy and speed of analog circuits that perform analog-to-digital and digital-to-analog conversion, amplification, filtering, and many other functions. Although the existence of such hysteresis was indicated in recent high-precision MOS analog circuits [1], no detailed measurement data have been available. In this paper, we describe extensive measurements of the threshold-voltage hysteresis in MOSFET's, under various conditions that emulate the normal operation of MOS analog circuits.

Manuscript received July 1, 1988; revised November 4, 1988. This work was supported by the National Science Foundation under Grant ECS-8505145 and by the Semiconductor Research Corporation under Grant 86-05-080.

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IEEE Log Number 8826143

In typical MOS analog circuits such as switched-capacitor filters [2], [3] or charge-redistribution A/D converters [1], [4], the differential inputs of operational amplifiers or comparators are subject to momentary asymmetrical voltage stresses during their normal operation. In comparators, the magnitude of the stress can be as large as half the full-scale voltage of the A/D converter, while in operational amplifiers, it can be on the order of the supply voltage under slewing conditions.

Charge-voltage hysteresis in MOS dielectrics can be caused by the drift of mobile ions [5], and by dipolar or interfacial polarization [6]. However, the time constants associated with these mechanisms are too long for them to be a serious source of error in typical data converters or switched-capacitor circuits which are reinitialized on time scales of 1–10 μs. The tunneling of channel charge carriers to traps in the oxide, on the other hand, leads to a large dispersion of time constants which can cause hysteresis effects at frequencies of interest in a wide variety of circuit applications.

There have been limited studies on MOS threshold-voltage hysteresis in the past. However, voltage, temperature, and time scales were far outside the normal operating range of modern integrated circuits [7]. In the present study, we examine threshold-voltage hysteresis due to oxide traps through its effect on the settling time of a differential amplifier operated at voltage and time scales relevant to typical analog integrated circuit applications.

## II. Theory

Traps located in the oxide close to the silicon–oxide interface can exchange carriers with the channel by tunneling. Electrons can either tunnel directly to oxide traps close to the conduction band or tunneling may occur via a two-step process in which carriers first communicate with fast surface states at the silicon–oxide interface and then tunnel at constant energy into traps in the oxide, or vice versa [8].

When an NMOS transistor is stressed at high positive gate–source voltage, the surface electron density increases and traps fill via the tunneling mechanisms. The bending of the oxide bands lowers trap energy levels with respect to the silicon bands so that they may be filled by either of these two tunneling mechanisms.

When the stress is removed, the band returns to the normal position, and the traps can empty back into the silicon. However, the rate at which traps empty is much slower than the rate at which they fill, because of the large difference in electron concentrations between filling and emptying processes. This asymmetry in the rates at which traps fill and empty can cause hysteresis in the threshold voltage of MOSFET's. Although the hysteresis will eventually decay as the traps empty, due to the long decay time (typically more than tens of milliseconds), the settling time of MOS circuits can be greatly affected.

If an NMOS device is subjected to a large positive gate voltage stress (i.e., a few volts), assuming acceptor type traps, the threshold voltage will increase. When the gate voltage returns to its initial condition, the drain current will not respond immediately, but will show some overshoot which settles to its final value with a long tail that persists during the time that the traps are returning to their steady-state occupancy.

Regardless of whether the tunneling occurs primarily from the conduction band or from fast surface states within the bandgap,

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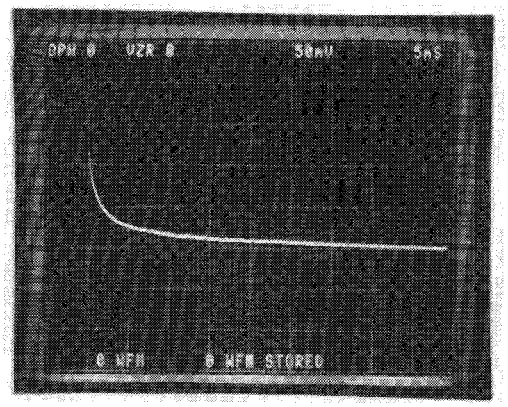


Fig. 1. Hysteresis in output voltage for an amplifier with 500/3 NMOS input transistors and a gain of 100 stressed for 1 ms at +5 V.

TABLE I
MEAN INPUT-REFERRED HYSTERESIS AND FLICKER NOISE AT 100 HZ, FOR THREE DIFFERENT 3-$\mu$m PROCESSES. HYSTERESIS WAS MEASURED AT A STRESS VOLTAGE OF 5 V FOR 1 ms.

| PROCESS | MEAN THRESHOLD VOLTAGE HYSTERESIS | INPUT REFERRED FLICKER NOISE (AT 100Hz) |
|---|---|---|
| 1 | 145 $\mu$V | 0.59 $\mu V/\sqrt{Hz}$ |
| 2 | 398 $\mu$V | 0.99 $\mu V/\sqrt{Hz}$ |
| 3 | 785 $\mu$V | 2.15 $\mu V/\sqrt{Hz}$ |

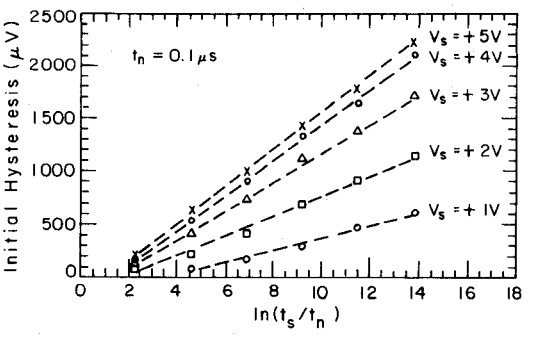


Fig. 2. Hysteresis in threshold voltage as a function of stress time with stress voltage as a parameter. $t_s$ is the stress time, and $t_n$ is a normalization time.

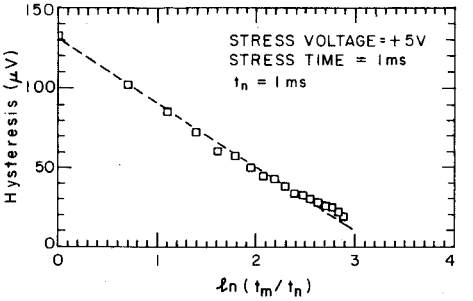


Fig. 3. Hysteresis in threshold voltage as a function of decay time.

it can be shown that the initial magnitude of the hysteresis is approximately a logarithmic function of the stress time $t_s$ [9]:

$$\Delta V_T(t_s) \approx A + B \ln t_s. \quad (1)$$

The coefficients in (1) depend on the trap density and the applied voltage. It can also be shown that the hysteresis decays approximately logarithmically with time.

## III. EXPERIMENTAL RESULTS

Actively loaded differential amplifiers with NMOS and PMOS input transistors at bias currents ranging from 10 to 500 $\mu$A were tested. The input transistors were 500 $\mu$m wide and 3 $\mu$m long for most of the process runs, while $100 \times 6$-$\mu m^2$ input devices were used in a 6-$\mu$m process run. The transconductance of the load transistors was made much smaller than that of the input transistors, so that the effect of hysteresis in the load transistors, if any, would be greatly reduced when referred to the input.

The input MOSFET's were stressed at voltages ranging from $-5$ to 5 V from their normal bias conditions, for times from 1 $\mu$s to 100 ms, and the hysteresis was observed on an oscilloscope. Drain-to-source voltages of the input transistors were kept under 0.5 V during stressing so that hot-electron effects did not affect the measurement. The hysteresis at the output of a typical differential amplifier with NMOS inputs and a voltage gain of approximately 100 is shown in Fig. 1. With a 5-V stress applied for 1 ms, the initial amplitude of the overshoot is about 1 mV referred to the input, and it decays with a long tail to its final value. A full 25 ms after the gate–source voltage has returned to its initial value, there is still an input referred error of over 100 $\mu$V. At 5-V 1-ms stress, the mean input-referred value of the hysteresis for NMOS transistors fabricated with 3-$\mu$m CMOS processes from three different foundries varied from 150 to 800 $\mu$V. Table I summarizes these results. A 6-$\mu$m CMOS process from a different foundry, which employed wet–dry–wet gate oxidation, showed as much as 1.2-mV mean hysteresis.

Fig. 2 shows the initial magnitude of hysteresis as a function of stress time with stress voltage as a parameter. The relation between stress time and hysteresis is very close to logarithmic, in agreement with the trapping theory. The hysteresis increases with stress voltage because more electrons are available for tunneling from the conduction band. The two-step mechanism also predicts an increase in hysteresis with stress voltage because the increase in surface potential and band-bending brings more traps within tunneling distance of filled surface states.

The magnitude of the hysteresis with time of measurement following stress is shown in Fig. 3. The decay is approximately logarithmic as is predicted by the theory.

Whereas positive stress voltages caused an overshoot and a long-tail decay in nearly all of the NMOS devices tested, the percentage of PMOS devices which exhibited any overshoot was significantly lower. Only a few isolated PMOS transistors showed measureable hysteresis. The initial amplitude of the overshoot was lower (on the order of 100 $\mu$V) and the decay time was comparable to the stress time, much shorter than for the NMOS devices. These results can be explained by differences in processing and band structures and electron and hole trapping [9].

Both NMOS and PMOS transistors exhibit negligible hysteresis for negative stress voltages. This suggests that hole trapping is much less probable than electron trapping.

Fig. 4 shows that the input-referred hysteresis decreases with bias current in the differential pair. At high bias currents, the surface is normally strongly inverted so that Fermi level becomes pinned. Additional positive gate stress causes minimal change of Fermi level, reducing the two-step tunneling process.

Since flicker noise is also caused by traps, it was measured in the same devices to find the correlation with the hysteresis. Table I shows a very strong correlation between the magnitude of hysteresis and flicker noise measured at 100 Hz.

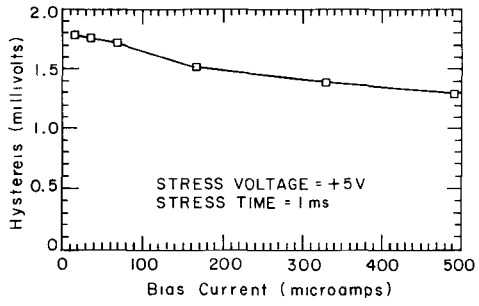


Fig. 4 Initial amplitude of input-referred hysteresis as a function of input transistor (500/3 NMOS) drain current.

## IV. Conclusions

NMOS transistors subjected to positive gate–source voltage transients exhibited 100 $\mu$V to more than 1 mV of input-referred hysteresis, depending on the stress conditions. PMOS transistors showed substantially less threshold-voltage hysteresis under the same test conditions. Negative gate stresses produced no measurable hysteresis in either channel type. This hysteresis effect was explained by a carrier tunneling/trapping theory. The theory predicted logarithmic dependence of hysteresis on the stress and decay time, which agreed well with the measurements. A strong correlation was found between hysteresis and flicker noise, supporting the theory.

Based on these findings, high-speed, high-accuracy analog circuits should be designed to avoid the conditions which lead to carrier trapping hysteresis. In particular, NMOS devices, especially on input stages, should not be subjected to large positive gate-to-source voltage transients. If possible at all, critical input stages should employ PMOS input transistors, which also improves flicker noise [10]. However, in general, the circuit speed will be reduced due to the lower transconductance available from PMOS input transistors.

## Acknowledgment

The authors wish to express their appreciation to Prof. S. D. Senturia, Prof. C. G. Sodini, and R. Jayaraman of the Massachusetts Institute of Technology for their helpful advice. They also thank S. English of Analog Devices for his help with the measurements and MOSIS for providing fabrication services.

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## Erratum to "A Fast Offset-Free Sample-and-Hold Circuit"

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Please note that in Fig. 2(a) on p. 1271 of the above paper,[1] nodes *A* and *B* were not marked. They are at the right-hand and left-hand terminals, respectively, of capacitor *C*.

Manuscript received November 7, 1988.

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IEEE Log Number 8926477

[1] F-J Wang and G C. Temes, *IEEE J. Solid-State Circuits*, vol. 23, no 5, pp. 1270–1272, October 1988