Oversampled Pipeline A/D Converters With Mismatch Shaping

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***Abstract*—This paper presents a pipeline analog-to-digital converter (ADC) with improved linearity. The linearity improvement is achieved through a combination of oversampling and mismatch shaping, which modulates the distortion energy out of band. Mismatch shaping can be realized in a traditional 1-bit/stage pipeline ADC, but the ADC's transfer characteristic properties limit its effectiveness at pushing the distortion out of band. These limitations can be alleviated by using a 1-bit/stage commutative feedback capacitor switching pipeline design. A test chip was fabricated in a 0.35-μm CMOS process to demonstrate mismatch shaping. Experimental results obtained indicate that the spurious-free dynamic range improves by 8.5 dB to 76 dB when mismatch shaping is used at an oversampling ratio of 4 and a sampling rate of 61 MHz. The signal-to-noise and distortion ratio improves by 3 dB and the maximum integral nonlinearity decreases from 1.8 to 0.6 LSB at the 12-bit level.**

***Index Terms*—Analog-to-digital converter, dynamic element matching, mismatch shaping, pipeline.**

I. Introduction

MANY applications, such as broadband communications, require high-speed and high-resolution ADCs. The signal bandwidths in these applications are increasing with new product generations, placing tough demands on the analog front ends. For example, the need to filter these wide-band signals prior to digitization to avoid aliasing of out-of-band signals requires the use of wide-band filters with narrow transition bands. These filters invariably have high orders and are difficult to design in practice. Although it is possible to oversample the input signal to relax the filtering requirements, this does demand higher sampling frequencies in the ADC. The wide bandwidth of the input signals limits the practically achievable oversampling ratios in current technology to between 4 and 8.

This work investigates the use of pipeline ADCs under these low oversampling conditions. In particular, it develops mismatch shaping (MS) algorithms for pipeline converters [1], [2]. MS, a technique developed for delta–sigma converters [3], pushes the distortion introduced by component mismatch out of the signal band, thereby improving the linearity. Unlike dynamic element matching [4] which spreads the distortion evenly over the entire Nyquist band, MS attempts to minimizes the distortion energy in the signal band.

The first part of this paper introduces MS algorithms for pipeline ADCs, along with the circuit implementation and simulation results. It also presents theoretical analysis which predict the behavior and provides insights into techniques to improve the performance. The second part describes the design of a test chip which was built as a vehicle to test the different MS algorithms. The experimental results are presented in the final section.

Manuscript received August, 2001; revised December, 2001. This work was supported in part by the Defense Advanced Research Projects Agency under contract DAAL-01-95-K-3526, and in part by Analog Devices, Compaq, IBM, Intersil, Lucent Technologies, Maxim Integrated Products, Multilink, National Semiconductors Company, Philips Research Laboratories, Silicon Laboratories, and Texas Instruments Incorporated.

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Publisher Item Identifier S 0018-9200(02)03661-2.

II. High-Performance ADCs at Low Oversampling Ratios

In recent years, a number of architectures have been proposed for applications where both high speed and high resolution are needed. These architectures include delta–sigma modulators, pipeline converters, and folding and interpolating converters. All of these architectures can be implemented in CMOS, however, folding and interpolating ADCs are better suited for bipolar or BiCMOS processes where transistors with good matching properties are available [5], [6].

Delta–sigma modulators are very popular ADCs in applications where high oversampling ratios are possible [7]. At high oversampling ratios, delta–sigma ADCs have many advantages compared with conventional ADCs. These advantages include:

- shaping of quantization noise, thereby reducing in-band quantization noise;
- ease of antialiasing due to oversampling;
- tolerance to component mismatches.

In delta–sigma converters employing a single loop and 1-bit feedback [7], the converter is inherently linear and hence does not require good component matching.

Delta–sigma converters with 1-bit feedback generally require a large oversampling ratio in order to achieve a high signal-to-noise ratio (SNR). This is because the order of the loop has a diminishing effect on the SNR for the loop to remain stable at high order [8]. The cascaded or MASH structure [9], [10] was developed to circumvent the instability of high-order delta–sigma converters, thus increasing the SNR at a given oversampling ratio. Unfortunately, the MASH is much less tolerant to component mismatches even when 1-bit feedback is used, because of quantization noise leakage. Moreover, the MASH is prone to limit-cycle tones which are unavoidable in low-order loops with 1-bit feedback. This makes MASH unsuitable for applications where a low oversampling ratio is desired.

Another method to increase the SNR of delta–sigma converters is to increase the number of bits in the feedback digital-to-analog (D/A) converter. An unfortunate consequence of multibit feedback is that the D/A converter must now be accurate to the final resolution of the delta–sigma converter. A number of techniques have been developed to overcome the accuracy problems in the multibit feedback ADCs. They include self-calibration [11], dynamic component matching [4], [12], and MS [3].

There have also been attempts at reducing the quantization noise over the entire Nyquist band, resulting in delta–sigma converters which do not require oversampling. This is accomplished either through parallel architectures [13] or pipeline architectures [14]. Both approaches rely on significantly increasing the analog hardware. Parallel architectures also suffer from path mismatches which need to be calibrated [15].

Pipeline converters have been traditionally applied to Nyquist-rate sampling. Although pipeline ADCs are relatively simple and power efficient, component mismatch limit the accuracy to about 10 bits. Numerous techniques which include self-calibration [16]–[19], error-averaging [20], ratio-independent [21] and reference refreshing [22] methods have been devised to remove errors due to component mismatch. Except for self-calibration techniques, all these techniques take up extra cycles of the valuable conversion time, reducing the throughput of the converter significantly and the added complexity often increases the power consumption considerably. Self-calibration techniques, on the other hand, remove component mismatch without increasing the conversion time. The drawback of self-calibration is the additional complexity and the necessity of the calibration period during which the converter is inoperable. The missing samples during this period can be generated using nonlinear interpolation [19], but this results in lower accuracy. Alternatively, redundant hardware can be used to avoid missing samples [23], but this inevitably increases power consumption and complexity. In practice, factory calibration has been preferred. However, to maintain calibration stability, the ADC errors must be completely dominated by capacitor errors over the entire life of the device [24].

In comparing delta–sigma converters and pipeline converters for wide-band signals, we recognize a few important attributes. Due to the wide bandwidth of the input signal and limited circuit speed, delta–sigma converters can afford only low oversampling ratios, which makes high-resolution conversion difficult. The required low oversampling ratio generally nullifies the primary advantage of delta–sigma converters: the tolerance to component mismatches. As for quantization noise in pipeline converters, the quantization noise can be made smaller by adding more stages at the end of the pipeline. Since the last stages of the pipeline do not contribute much thermal noise, they can be made extremely small and low power. Therefore, the quantization noise itself can be made arbitrarily small with negligible increase of area and power.

Based on the above observations, we can conclude that delta–sigma converters are not fundamentally advantageous over pipeline converters for wide-band applications that necessitate low oversampling ratios. At these low oversampling ratios, the benefits of delta–sigma modulation tend to disappear.

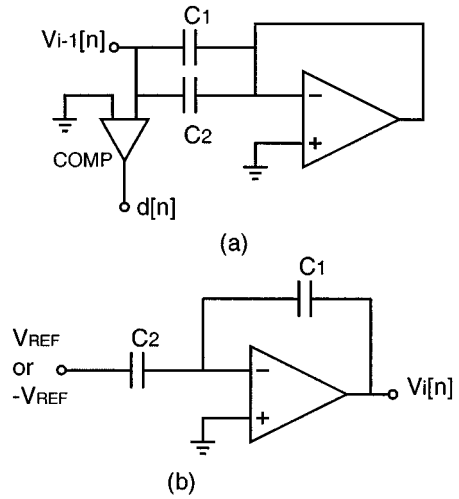

Fig. 1. The ith stage of a 1-bit/stage pipeline ADC.

Two delta–sigma designs have been reported at oversampling ratios of 4 to 8 [25], [26]. The design of these converters involves the linearization of multibit DACs and is complex. Although the complexity can perhaps be reduced if lower SNR figures are desired by reducing the number of bits in the DAC, the number of bits cannot be reduced to 1 where no dynamic element matching would be needed, mainly to avoid integral nonlinearity [4] and instability.

We propose the simple approach of oversampling a pipeline converter and shaping the mismatch distortion out of band, where it will be removed by a subsequent digital filter. Since no attempt is made to shape the quantization noise, there are none of the concerns associated with delta–sigma converters with a low oversampling ratio.

In addition to simplicity, a pipeline design offers some interesting advantages from a system design perspective. First, a pipeline design can be easily reconfigured to perform Nyquist conversion using the same hardware. Second, pipeline converters offer a simple way to save power under operating conditions where the full resolution is not needed, through powering down and bypassing unneeded front-end stages [27]. In a 1-bit/stage implementation, the granularity of this power-resolution control is very fine, allowing for flexibility in system optimization. Finally, since the pipeline converter is fundamentally a memoryless system, it can be easily multiplexed. This allows for the same ADC to digitize multiple input channels, while oversampling and mismatch shaping each one of them.

III. Mismatch Shaping in Traditional 1-Bit/Stage Pipeline Converters

An N-bit 1-bit/stage pipeline converter is composed of a cascade of N stages. Each stage contributes a single bit to the digital output. The implementation of the ith stage is shown in Fig. 1. The capacitors C_1 and C_2 are nominally identical. Each stage operates in two phases, a sampling phase and a multiplying phase. During the sampling phase shown in Fig. 1(a), both C_1 and C_2 sample the input voltage to the stage $V_{i-1}[n]$. At the

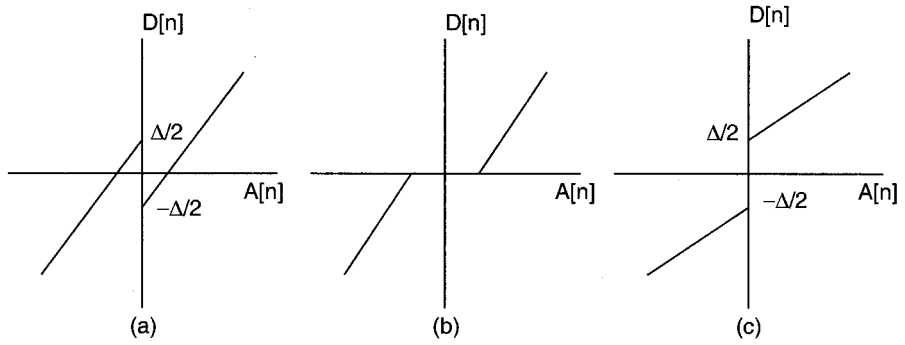

Fig. 2. Effects of the first stage capacitor mismatch ($V_{\rm REF} = 1$). a) $\Delta < 0$. b) $\Delta < 0$ and no digital error correction results in a wide code. c) $\Delta > 0$.

same time, the comparator determines whether the input voltage $V_{i-1}[n]$ is greater than or less than 0 V.

If $V_{i-1}[n] > 0$, then the stage decision bit $d[n] = 1$, otherwise $d[n] = 0$. During the second phase, which is the amplifying phase, C_1 is connected to the output of the operational amplifier and C_2 is connected to either the reference voltage $V_{\rm REF}$ or $-V_{\rm REF}$, depending on the bit value $d[n]$. If $d[n] = 1$, C_2 is connected to $V_{\rm REF}$, resulting in an output voltage

$$V_i[n] = 2V_{\rm in}[n] - V_{\rm REF}. \tag{1}$$

Otherwise, C2 is connected to $-V_{\rm REF}$, giving an output voltage

$$V_i[n] = 2V_{\rm in}[n] + V_{\rm REF}. \tag{2}$$

In other words

$$V_i[n] = 2V_{\rm in}[n] + (-1)^{d[n]}V_{\rm REF}. \tag{3}$$

In practice, a number of sources introduce errors in the conversion [18], [28]. They include the charge injection from the sampling switch, the comparator offset, and the mismatch between C_1 and C_2. We assume here that the open-loop gain of the operational amplifier is sufficiently large. By employing the standard digital error correction, the comparator offset can be easily compensated [29]. The effect of charge injection can be substantially reduced by a fully differential configuration and bottom-plate sampling. The residual charge injection causes only a benign input-referred offset of the converter with digital error correction. The effect of capacitor mismatch, however, is much more difficult to remove. If we define

$$C = \frac{C_1 + C_2}{2} \tag{4}$$

$$\Delta = \frac{C_1 - C_2}{C} \tag{5}$$

then the resulting output voltage $V_i[n]$ can be shown to be

$$V_i[n] \approx 2\left(1 - \frac{\Delta}{2}\right)V_{i-1}[n] + (-1)^{d[n]}(1-\Delta)V_{\rm REF}. \tag{6}$$

In order to consider the effect of the capacitor mismatch on the converter characteristic, assume that only the first stage of the pipeline has the capacitor mismatch Δ and all subsequent stages have perfect matching. From (6), we can write the input-referred converter characteristic as

$$D[n] \approx \begin{cases} A[n]\left(1 - \dfrac{\Delta}{2}\right) + V_{\rm REF}\dfrac{\Delta}{2} & \text{if } A[n] > 0 \\ A[n]\left(1 - \dfrac{\Delta}{2}\right) + V_{\rm REF}\dfrac{\Delta}{2} & \text{otherwise} \end{cases}$$

where $A[n]$ and $D[n]$ are the converter input and output, respectively. The resulting converter characteristic is indicated in Fig. 2. The nonmonotonicity near the center of the characteristic in Fig. 2(a) for $\Delta < 0$ arises if digital error correction is employed in the subsequent stages. Otherwise, a "wide code" will result as shown in Fig. 2(b). When $\Delta > 0$, then missing codes result as shown in Fig. 2(c).

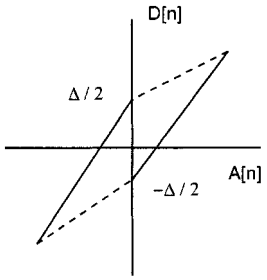

Fig. 3. Mismatch shaping applied to a 1-bit/stage pipeline ADC results in alternating between the two transfer characteristics ($V_{\rm REF} = 1$).

A. Rudimentary Mismatch Shaping

As rudimentary MS, one can exchange the roles of C_1 and C_2 at the sampling rate. In other words, for one sample of the input, C_1 and C_2 are operated as shown in Fig. 1. For the next sample, C_2 is employed as the feedback capacitor while C_1 is connected to $V_{\rm REF}$ or $-V_{\rm REF}$. The converter characteristic will alternate at the sampling frequency between that in Fig. 2(a) and 2(c), as shown in Fig. 3, if digital error correction is employed. We see that although the amplitude of the error introduced into each sample is the same as before, the polarity of the error now alternates. MS has simply multiplied the distortion by -1^n and hence modulated it to half the sampling frequency. If the analog input is dc, the error is modulated to half the sampling rate and can be removed completely by a digital low-pass filter. Since the MS is to be applied to oversampled converters, the input does not change very rapidly from one sample to another, and we

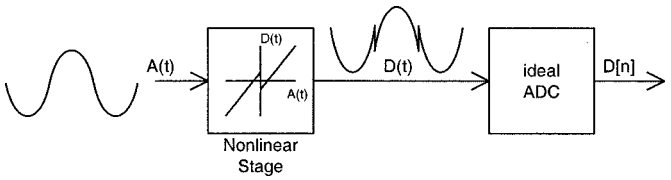

Fig. 4. Converter model used for distortion analysis.

Fig. 5. Converter nonlinearity output decomposition.

can reason that most of the distortion will be pushed out to high frequencies.

B. Performance Analysis

To get a quantitative estimate of the performance of this MS technique, let us assume that the input to the ADC is a single tone $A(t) = A\cos(\omega t)$. Furthermore, let us assume that the capacitors mismatch only in the first pipeline stage resulting the transfer characteristics of Fig. 3. To calculate the distortion spectrum that will result when no MS is applied, we can assume that the input first goes through a continuous-time nonlinear stage which models the ADC nonlinearity, followed by an ideal ADC as shown in Fig. 4. The output of the nonlinearity $D(t)$ can be decomposed into the sum of a sinusoid and a square wave with a peak to peak amplitude of Δ, as illustrated in Fig. 5. A Fourier series expansion of the square wave reveals that it has frequency components at odd multiples of the input frequency, each with an amplitude equal to $A_i = 2\Delta/\pi i$, where i is an odd integer representing the harmonic number. When $D(t)$ is digitized by the ideal ADC, the distortion components in $D(t)$, which are at frequencies above half the sampling frequency, fold back into the frequency band from 0 to half the sampling frequency. This is illustrated in Fig. 6(a), which shows the simulated output spectrum for a 15-bit converter with 0.1% mismatch in the first stage and a full scale input. The dominant harmonics in this spectrum fall as $1/i$.

When MS is applied, the distortion is modulated to half the sampling frequency as shown in Fig. 6(b). Since the oversampling ratio is low and the dominant distortion components only fall off as $1/i$, strong distortion components alias back into the signal band. For example, at an oversampling ratio of 4, the worst-case scenario is when the input is a single input tone at the edge of the signal band. This results in the fifth harmonic falling in the signal band, and the improvement in the spurious-free dynamic range (SFDR) due to MS is only 4.4 dB. At an oversampling ratio of 8, the worst case results in the ninth harmonic falling in-band which leads to a 9.5-dB improvement in SFDR.

IV. Mismatch Shaping Using the CFCS Pipeline ADC

To improve the performance of the MS technique described in the last section it is desirable to use an ADC which will introduce distortion components that fall faster than $1/i$. To help toward that goal, one can try to eliminate jump discontinuities in the transfer characteristic of the converter to make it smooth. The converter characteristic in Fig. 8 can be obtained by the commutative feedback capacitor switching (CFCS) in [30]. CFCS is implemented by slightly altering the basic operation of the standard converter shown in Fig. 1. Instead of designating C_1 as the feedback capacitor, either C_1 or C_2 is selected as the feedback capacitor while the other capacitor is connected to $V_{\rm REF}$ or $-V_{\rm REF}$ depending on the bit value $d[n]$. The sampling phase shown in Fig. 7(a) is unchanged. For $d[n] = 1$, the operation is the same as in Fig. 1, with C_1 being selected as the feedback capacitor. For $d[n] = 0$, however, C_2 is selected as the feedback capacitor as shown in Fig. 7(c). It is shown in [30] that this operation gives the characteristic in Fig. 8 despite capacitor mismatches. The dotted characteristic in Fig. 8 with the errors in the opposite direction can be obtained by reversing the roles of C_1 and C_2; For $d[n] = 1$, C_2 is selected as the feedback capacitor and for $d[n] = 0$, C_1 is selected as the feedback capacitor. Alternating between these two characteristics at the sampling rate pushes the mismatch error to high frequencies.

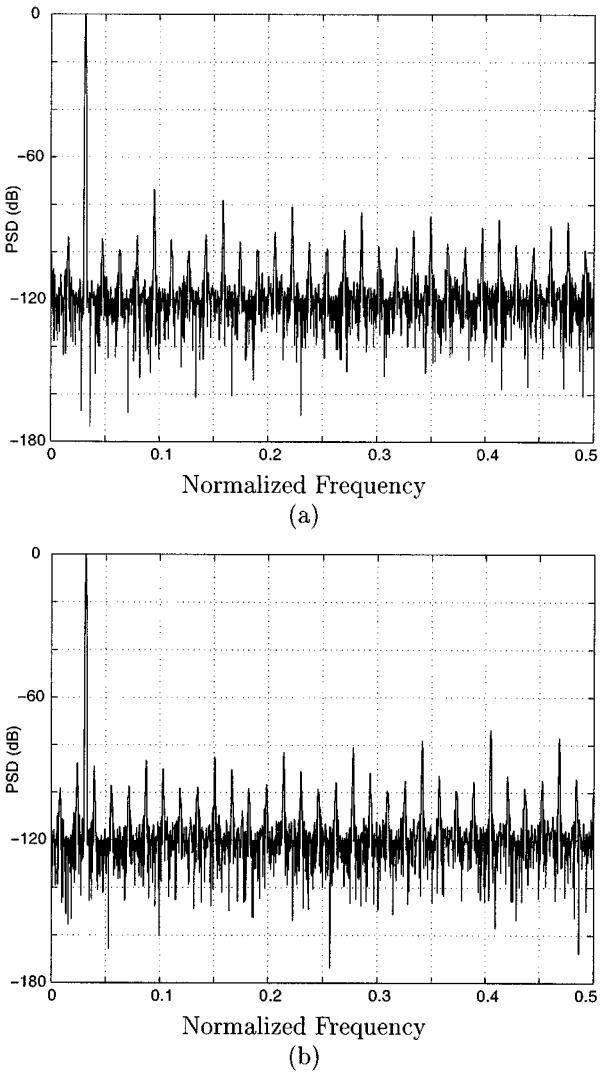

Fig. 6. Simulated power spectral density of the output of a traditional 1-bit/stage 15-bit pipeline ADC with 0.1% mismatch in the first stage. a) Without mismatch shaping. b) With mismatch shaping.

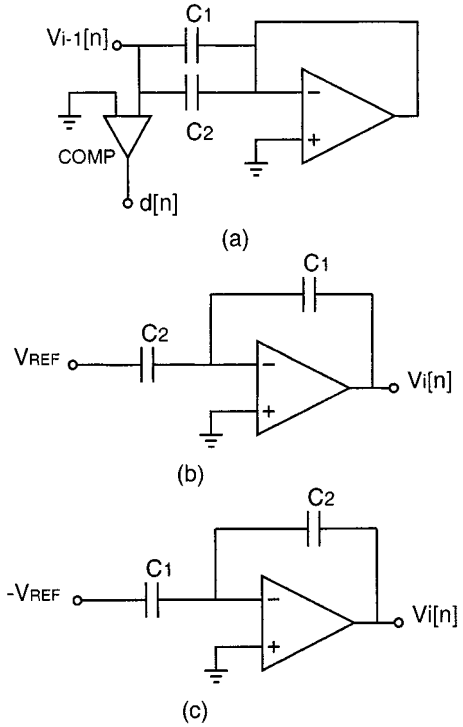

Fig. 7. Commutative feedback capacitor scheme (CFCS).

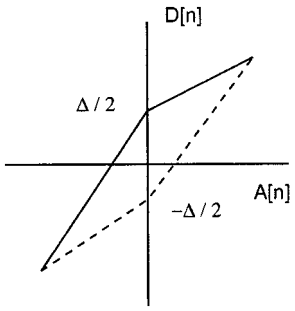

Fig. 8. CFCS converter transfer characteristic with Δ mismatch only in the first stage ($V_{\rm REF} = 1$).

In addition to the reduced differential nonlinearity (DNL) [30], the 1-bit-per stage CFCS ADC has a transfer characteristic with a nonlinear portion which is even. That is, the integral nonlinearity (INL) is even.

If we assume capacitor mismatch only in the first stage of the pipeline, as defined in (4) and (5), then the transfer characteristic of the converter can be found using an approach similar to the one used in the last section and will equal

$$D[n] \approx \begin{cases} A[n]\left(1-\dfrac{\Delta}{2}\right)+V_{\rm REF}\dfrac{\Delta}{2}, & \text{if } A[n]>0 \\ A[n]\left(1+\dfrac{\Delta}{2}\right)+V_{\rm REF}\dfrac{\Delta}{2}, & \text{otherwise} \end{cases}$$

as shown in Fig. 8. Separating the linear and nonlinear parts gives

$$D[n] \approx A[n] + V_{\rm REF}\frac{\Delta}{2} - \|A[n]\|\frac{\Delta}{2}. \tag{7}$$

The nonlinear part is the absolute value function and is an even function.

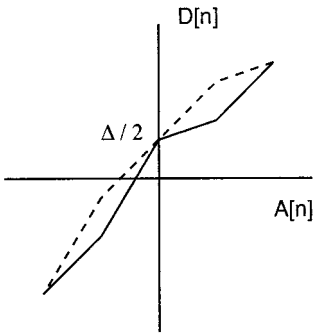

Fig. 9. Effect of capacitor mismatch in the first two stages of a pipeline on the input–output characteristic of a CFCS converter ($V_{\rm REF} = 1$).

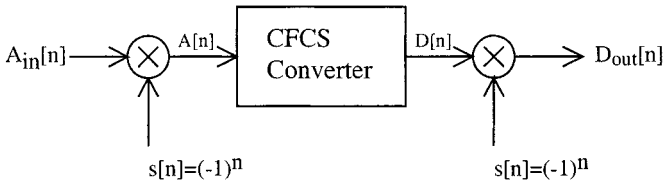

Fig. 10. Simple implementation of mismatch shaping using a 1-bit-per stage CFCS ADC.

When the first two stages of the pipeline suffer from capacitor mismatch, each linear segment of Fig. 8 will be replaced by a segment with the overall shape of Fig. 8, resulting in the transfer characteristic shown in Fig. 9. The effect of mismatch in the remaining stages of the pipeline can be found by repeating this process for each linear segment. Due to the even symmetry of this replacement process, the nonlinear portion of the converter transfer characteristic maintains an even symmetry, even with capacitor mismatch in all the ADC stages. The dashed line in Fig. 9 can be achieved by reversing the role of C_1 and C_2 in the second pipeline stage.

A. A Simple Implementation of Mismatch Shaping Using a CFCS ADC

A simple implementation of MS using a CFCS ADC is shown in Fig. 10. If the input to the CFCS is multiplied by -1 at alternating sampling phases and its digital output is also multiplied by -1 during those phases, as shown in Fig. 10, then the converter characteristics simply alternates between the characteristics in Fig. 8 at a rate equal to the sampling frequency, and MS is realized. To understand this, let us analyze the implementation in Fig. 10. The CFCS converter characteristic can be expressed as

$$D[n] = A[n] + N_w[n] + N_{1/f}[n] + g(A[n]) \tag{8}$$

where $A[n]$ and $D[n]$ are the input and output of the CFCS ADC, respectively. $N_w[n]$ is the ADC white noise, which includes quantization and thermal noise. $N_{1/f}$ is the converter $1/f$ noise. The function $g(.)$ models the nonlinearity of the ADC, which is a result of the capacitor mismatch in the stages of the pipeline. The CFCS ensures that $g(.)$ does not contain any large discontinuities which would result in differential nonlinearity. In addition, it ensures that $g(.)$ is an even function. The input of the

ADC $A_{\text{in}}[n]$ is multiplied by a sequence $s[n] = (-1)^n$, resulting in $A[n] = A_{\text{in}}[n]s[n]$. Then $A[n]$ is digitized by the CFCS core resulting in

$$D[n] = s[n]A_{\text{in}}[n] + N_w[n] + N_{1/f}[n] + g\left(A_{\text{in}}[n]\right). \quad (9)$$

This result can be obtained by noting that $g(x_{\text{in}}s[n]) = g(x_{\text{in}})$, because $g(.)$ is an even-order function. Finally, the output of the CFCS core is multiplied by the same sequence $s[n]$ giving

$$D_{\text{out}}[n] = A_{\text{in}}[n] + s[n]N_w[n] + s[n]N_{1/f}[n] + s[n]g\left(A_{\text{in}}[n]\right). \quad (10)$$

The first term in $D_{\text{out}}[n]$ is the desired signal $A_{\text{in}}[n]$. The second term, $s[n]N_w[n]$, is the quantization and thermal noise modulated to half the sampling frequency π, an operation that does not change its white nature. The third term, $s[n]N_{1/f}[n]$, is the $1/f$ noise modulated to half the sampling frequency, and hence MS removes the $1/f$ noise from the band of interest. The final term is the distortion components modulated to half the sampling frequency π.

From the above analysis, it is evident that a CFCS core with its even INL is essential for this scheme to work. If a converter with odd INL is used, then $g(x_{\text{in}}s[n]) = s[n]g(x_{\text{in}})$ and the input will pass through the same characteristic during all sampling phases and the distortion will not be modulated to half the sampling frequency.

In a fully differential implementation multiplying the input with ± 1 can be realized by swapping the polarity of the input applied to the CFCS stage, an operation which has a very simple circuit realization. The multiplication by ± 1 in the digital domain can also be realized very simply. Moreover, the implementation of the 1-bit/stage CFCS pipeline converter only requires a very slight modification of the standard pipeline stage comparator's logic, to give the even nonlinearity. It can be concluded, therefore, that the circuit implementation of this technique entails only little added complexity. Although a digital low-pass filter is needed to remove the out-of-band distortion, this filter would serve the dual purpose of augmenting the function of the weak analog antialiasing filter.

B. Performance Analysis

We can analyze the distortion in the output of the CFCS converter using the model of Fig. 11, in an approach similar to the one used in the last section. With a sinusoidal input $A(t) = A\cos(\omega t)$ and no MS, the output of the nonlinearity, $D(t)$, can be decomposed into a sinusoidal signal plus a full wave rectified sinusoidal with a peak value of ΔA, as shown in Fig. 12. A Fourier series expansion of the full wave rectified sinusoid reveals that it contains even-order distortion components with an amplitude $A_i = (2\Delta A)/\pi(i^2 - 1)$, where i is an even integer representing the harmonic number and A is the amplitude of the input. The ideal ADC causes frequency folding, as plotted in Fig. 13(a) for a 15-bit CFCS ADC with 0.1% mismatch in the first stage and a full-scale input. The dominant distortion components fall as $1/i^2$. When MS is applied, the distortion is modulated to half the sampling frequency, and since the harmonics fall as $1/i^2$, significant improvement in SFDR can be expected, as can be seen in Fig. 13(b). For example, at an oversampling ratio of 4, under the worst-case scenario, the fourth harmonic will alias in-band when MS is used, yet this represents a 14-dB improvement in SFDR over a nonmismatch-shaped CFCS ADC. Moreover, this represents a 9.5-dB improvement over a non-CFCS mismatch-shaped pipeline converter operating at the same oversampling ratio.

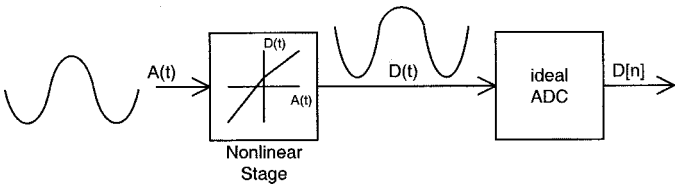

Fig. 11. Converter model used for distortion analysis.

Fig. 12. Converter nonlinearity output decomposition ($A = 1$).

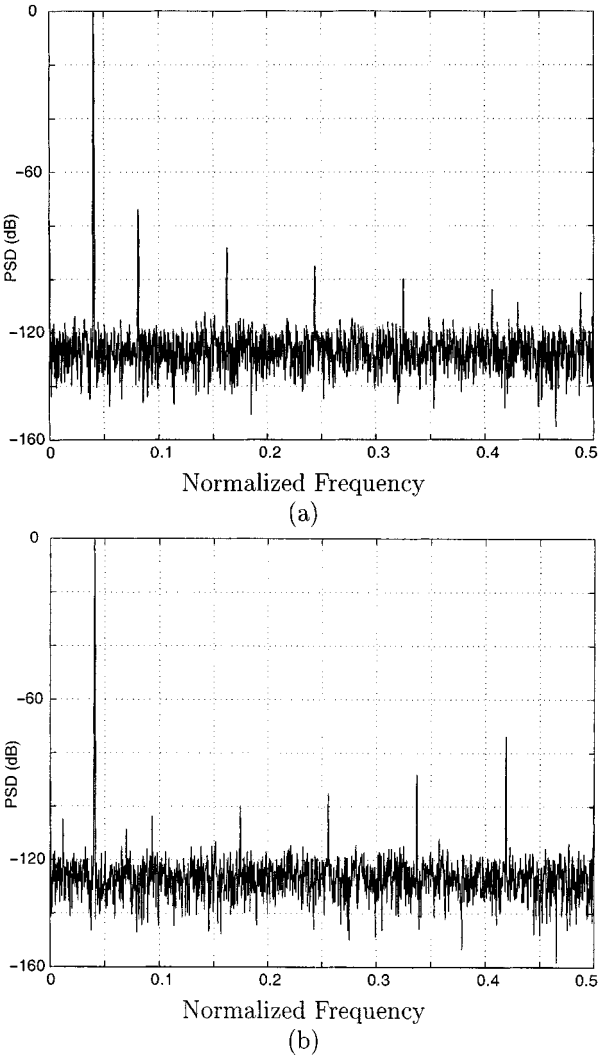

Fig. 13. Power spectral density (PSD) of the output of a 15-bit CFCS ADC with 0.1% mismatch in the first stage and a 1-bit/stage architecture. a) Without mismatch shaping. b) With mismatch shaping.

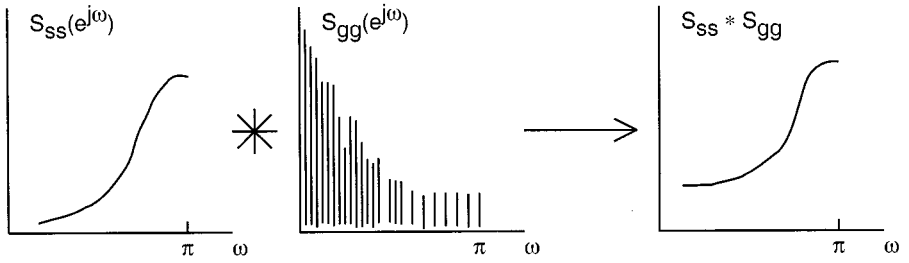

Fig. 14. The PSD of the swapping sequence needs to have most of its energy concentrated at half the sampling frequency to effectively whiten the in-band tones and realize mismatch shaping.

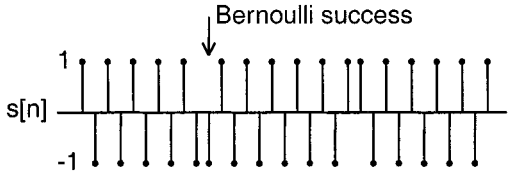

Fig. 15. The swapping sequence has phase jumps at every Bernoulli counting process increment.

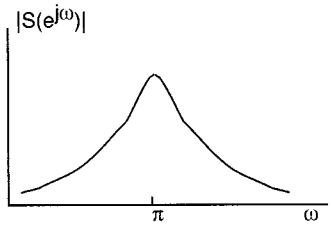

Fig. 16. PSD of swapping sequence.

C. Choice of Sequences for $s[n]$

To gain a further insight on how to improve the performance of the ADC, let us revisit (10). Modulating the distortion components $g(A_{\mathbf{in}}[n])$ to half the sampling frequency using $s[n] = (-1)^n$ does not eliminate discrete harmonic tones in the signal band, but it does reduce their amplitude. To randomize the in-band harmonics, a random swapping sequence can be used instead of $s[n] = (-1)^n$. The power spectral density (PSD) of this sequence must satisfy a few requirements, in order to effectively eliminate tones and to simultaneously achieve MS. In the frequency domain, the spectrum of the swapping sequence $S_{ss}(e^{j\omega})$ is convolved with the spectrum of the distortion $S_{gg}(e^{j\omega})$. For the result of the convolution $(S_{ss}(e^{j\omega})^* S_{gg}(e^{j\omega}))$ to be spectrally shaped with most of its energy concentrated at half the sampling frequency and with a randomized in-band noise floor, it is desirable for $S_{ss}(e^{j\omega})$ to have a single PSD lobe at half the sampling frequency. In addition, the PSD lobe of $S_{ss}(e^{j\omega})$ should be wide enough to spread the in-band distortion tones as shown in Fig. 14, but not too broad, to prevent a rise in the in-band noise floor.

A candidate sequence with many of the desired PSD properties is

$$s[n] = (-1)^{n+B[n]} \tag{11}$$

where $B[n]$ is a discrete-time Bernoulli counting process, a process that increments with every Bernoulli success event [31]. We can write $B[n] = \sum_{i=0}^{n} b_i$, where b_i is an independent Bernoulli trial which equals 1 with probability α and zero with probability $1 - \alpha$. In the time domain, $s[n]$, shown in Fig. 15, looks like a phase modulated alternating sequence, with 180° phase jumps occurring at every Bernoulli success.

The PSD of $s[n]$ decays away from half the sampling frequency as illustrated in Fig. 16 for $\alpha \in (0, 0.5)$. The rate of decay can be increased by reducing α, which helps in reducing the energy of $s[n]$ at low frequencies, but results in a narrower PSD bandwidth. Conversely, attempting to increase the bandwidth of the PSD lobe results in an increase of the energy at low frequencies. The value of α needs to be optimized to simultaneously satisfy these conflicting requirements.

The main shortcoming of using a noise-shaped sequence is that it can degrade the ADC's SNR. This degradation in performance can be understood by noting that one component of the ADC noise floor results from convolving the spectrum of the distortion with the spectrum of the swapping sequence. If the core ADC in Fig. 10 produces strong distortion components, even if they are primarily low-order distortion components, the convolution will inevitably result in a rise in the total in-band noise floor. Simulation results will demonstrate this in the next section.

D. Simulation Results

To demonstrate the previous MS algorithms, a MATLAB program was written to model the behavior of a 1-bit/stage CFCS pipeline converter. The model contains 15 pipeline stages. The first stage produces 1-bit, while the remaining stages produce 2-bits/stage to allow for digital error correction.

Fig. 17 shows the converter output spectrum when no MS is applied for an oversampling ratio (OSR) of 4. Strong distortion components fall in-band, limiting the signal-to-noise and distortion ratio (SNDR) to 72.8 dB and the SFDR to 70 dB for an OSR of 4. When MS is applied using a sequence $s[n] = (-1)^n$, the spectrums shown in Fig. 18 results and the distortion is modulated to half the sampling frequency, improving the SNDR to 80.8 dB and the SFDR to 84 dB for an OSR of 4. When $s[n]$ is a noise-shaped sequence with a PSD shown in Fig. 20, then the output spectrum of Fig. 19 results. The in-band distortion components are whitened and SFDR improves to 97 dB for an oversampling ratio of 4. The overall noise floor does rise in this case as anticipated, resulting in a SNDR of 79.6 dB. All these results were obtained with 0.1% capacitor mismatch in all the pipeline stages. Moreover, the polarity of the mismatch error in each stage was selected to give the worst-case performance. The results are summarized in Table I, which also shows the result obtained at an OSR of 8.

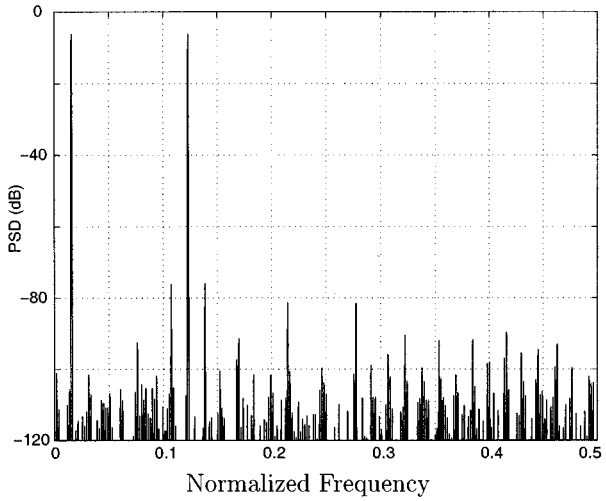

Fig. 17. The PSD of the output of a 15-bit CFCS ADC with 0.1% mismatch in all pipeline stages without mismatch shaping at an OSR $= 4$.

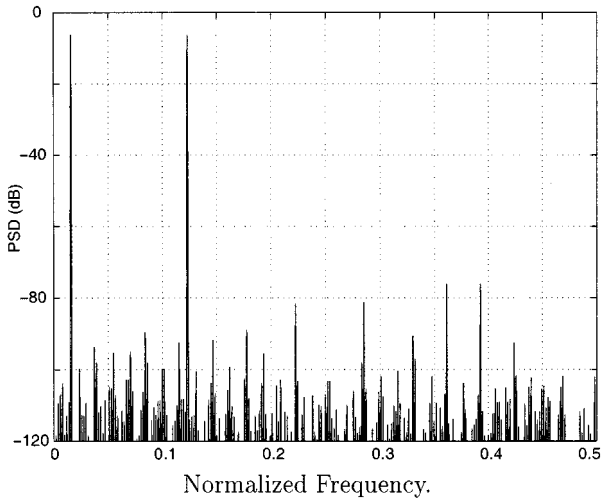

Fig. 18. The PSD of the output of a 15-bit CFCS ADC with 0.1% mismatch in all pipeline stages with mismatch shaping using $s[n] = (-1)^n$ at an OSR $= 4$.

E. Impact of Nonidealities

The techniques presented in this section hinge on the even nature of the INL characteristic of the 1-bit/stage CFCS converter, which is the result of capacitor mismatch. Practically, the INL will also contain a small amount of odd terms due to effects such as finite opamp gain, input dependent charge injection, incomplete settling and comparator offsets. The distortion introduced due to these mechanisms will not be pushed out-of-band using MS and will impact the linearity of the converter. Fortunately, the impact of these nonidealities can be minimized through careful circuit design to the extent that is required by the application at hand. It is worth noting that opamp offsets can be referred to the ADC input as an overall offset and will be removed by MS.

The transfer characteristic of a CFCS ADC in the absence of capacitor mismatch, but with the first pipeline stage opamp

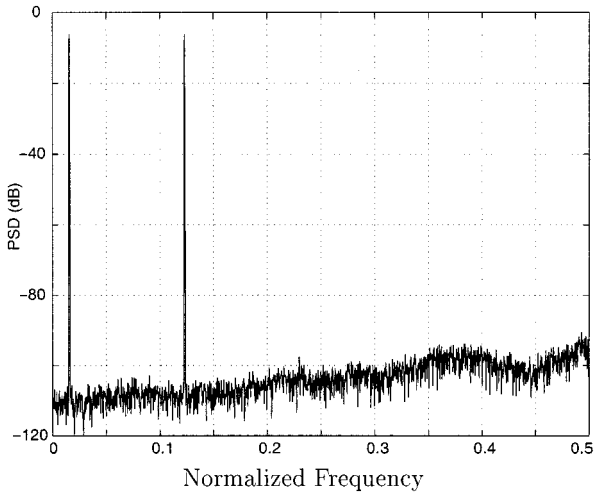

Fig. 19. The PSD of the output of a 15-bit CFCS ADC with 0.1% mismatch in all pipeline stages with mismatch shaping and $s[n]$ is a noise-shaped sequence in Fig. 20 at an OSR $= 4$.

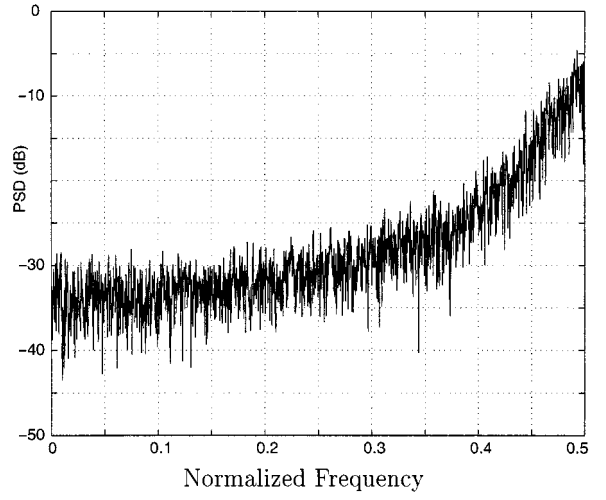

Fig. 20. The PSD of the noise shaped sequence $s[n]$ used to obtain the results in Fig. 19.

TABLE I
SUMMARY OF SIMULATED PERFORMANCE

Algorithm	OSR=4 SNDR(dB)	OSR=4 SFDR(dB)	OSR=8 SNDR(dB)	OSR=8 SFDR(dB)
CFCS	72.8	70	72.8	70
$s[n] = (-1)^n$	80.8	84	91.1	94
$s[n]$ in Fig. 20	79.6	97	86	103

having a gain of G, can be found using the same analysis method used earlier to be

$$D[n] = \begin{cases} A[n]\dfrac{1}{1+\frac{2}{G}} + \dfrac{V_{\text{REF}}}{2+G} & \text{if } A[n] > 0 \\ A[n]\dfrac{1}{1+\frac{2}{G}} - \dfrac{V_{\text{REF}}}{2+G} & \text{otherwise.} \end{cases}$$

As the gain of the opamp is increased, the nonlinearity introduced into the transfer characteristic will be reduced and its impact on the SNDR of a mismatch shaped converter will be reduced as plotted in Fig. 21. The improvement does saturate at high gain values because the SNDR becomes dominated by the

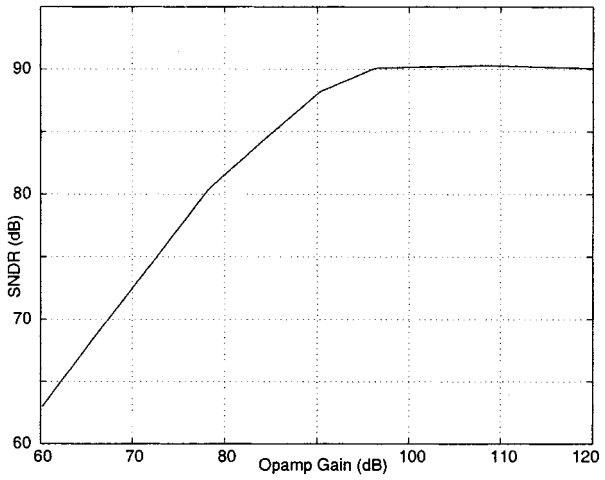

Fig. 21. SNDR versus opamp gain for a mismatch-shaped CFCS ADC with 0.1% capacitor mismatch and finite opamp gain in all pipeline stages.

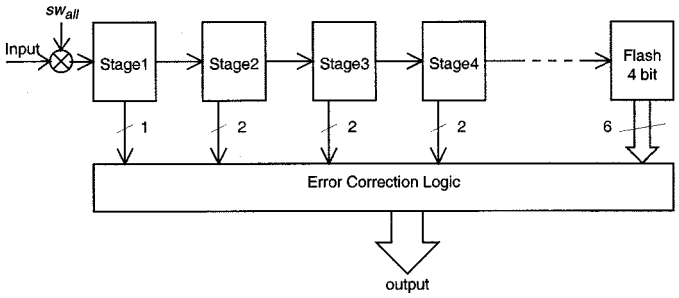

Fig. 22. ADC block diagram.

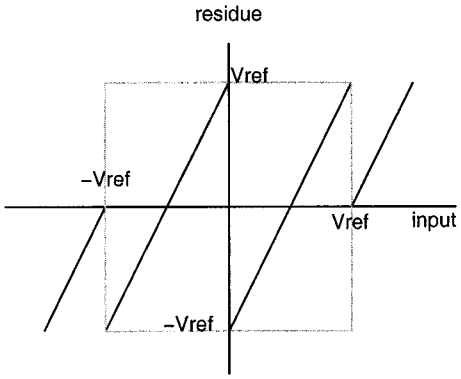

Fig. 23. Residue diagram for the pipeline stages following the first stage.

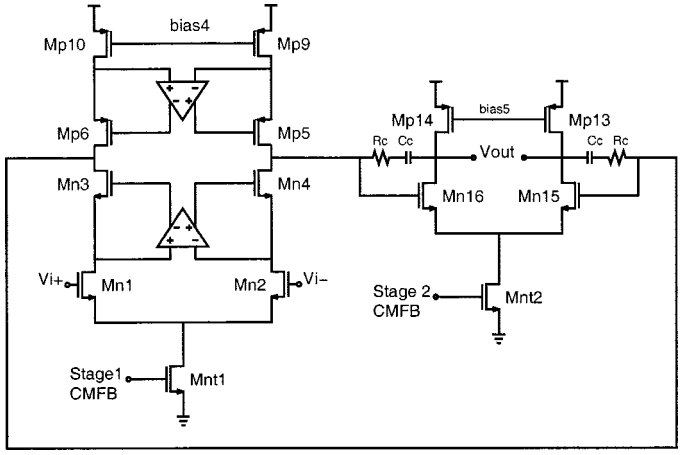

Fig. 24. Simplified circuit diagram of the opamp.

tones due to capacitor mismatch which alias back into the signal band.

The effect of comparator offset on the transfer characteristic is different than opamp gain. With capacitor mismatch in the first pipeline stage, the transfer characteristic can be rewritten with threshold between the two line segments of the transfer characteristic set to $V_{\rm os}$. Simulations indicate that an offset as large as 5% of the reference voltage $V_{\rm REF}$ can be tolerated without degrading the effectiveness of mismatch shaping. This does assume that the pipeline stage opamp does not saturate when its output exceeds $V_{\rm REF}$ because of the comparator offset. Digital error correction will not function properly if the opamp saturates, and this will result in missing and wide codes.

V. ADC Architecture

Fig. 22 shows the ADC block diagram. The ADC is composed of eleven CFCS pipeline stages, a back-end flash ADC, digital error correction logic, and a front-end multiplier for mismatch shaping using the sequence $sw_{\rm all}$. The front-end multiplier is implemented using cross-coupled nMOS transistor switches, which are part of the first-stage sampling network. A back-end multiplier is also needed, but is implemented off-chip in software.

Although the ADC has a resolution of 12 bits, it produces a 15-bit output. This reduces the quantization noise to a level much below the $(KT)/C$ thermal noise floor. This allows us to increase the thermal noise budget by reducing the values of the capacitors used and hence save power.

The first stage produces a single bit, whereas stages 2 through 11 produce 2 bits each, to allow for digital error correction [29]. Fig. 23 plots the residue diagram for stage 2, which is identical to the residue diagram for the remaining pipeline stages. The design of the CFCS pipeline stages is fully differential and is based on the principle explained in the previous section. The final stage in the pipeline is a 4-bit flash ADC, which also outputs two additional bits to be used for digital error correction.

For 12-bit performance with a 1.4-V signal swing and an OSR of 4, 250-fF capacitors are used in the first stage of the pipeline. This value gives a $(KT)/C$ thermal noise floor low enough to achieve a 67-dB SNR at an OSR of 4. The sampling capacitors and the opamps are scaled down by a factor of two in stages 2, 3, and 4 to save power. Continuing to scale beyond the fourth stage would result in extremely small capacitors and was therefore avoided.

The two-stage design shown in Fig. 24 was chosen for the opamp. A single-stage opamp design is not a possible candidate for a high-speed converter operating at a supply voltage of 3.3 V, simply because the opamp will have a very small output swing. A telescopic amplifier with regulated cascode gain enhancement is used for the first stage. The second stage has a tail transistor in order to accommodate the large common-mode voltage at the output of the first stage. Only nMOS devices are used in the signal path to enhance the speed [32]. The common-mode levels

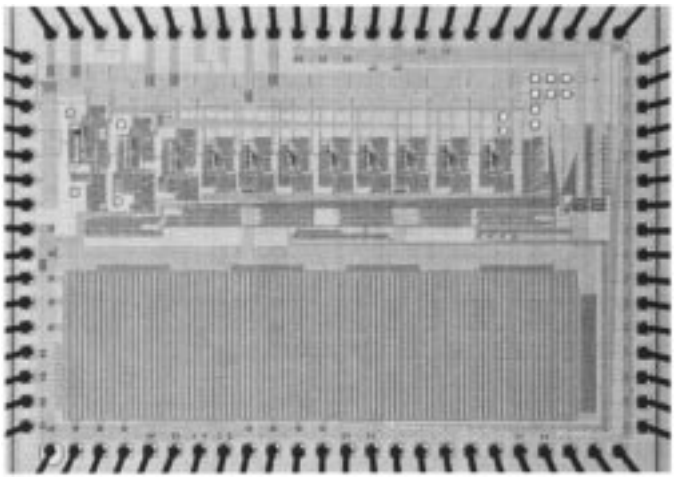

Fig. 25. Test chip microphotograph.

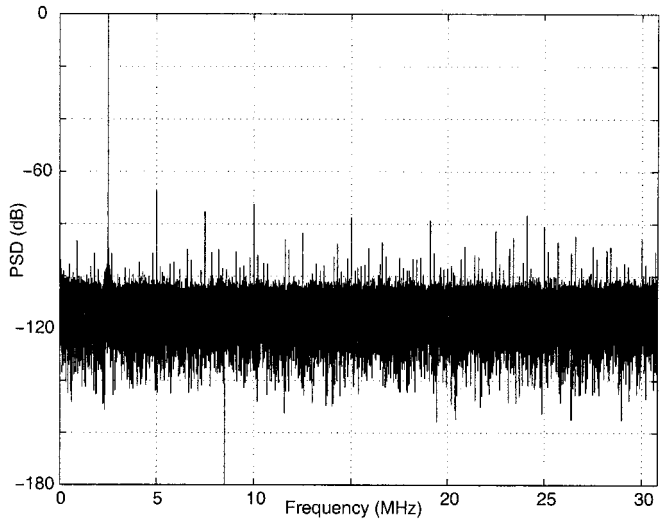

Fig. 26. CFCS ADC: SNDR $= 64.1$ dB, SFDR $= 67.5$ dB, $f_s = 61.6$ MHz, $f_{\rm in} = 2.5$ MHz, and OSR $= 4$.

in the opamp are regulated using two independent loops, one for each stage.

VI. Experimental Results

Fig. 25 shows the microphotograph of the test chip described in the last section, which was fabricated in TSMC's 0.35-μm CMOS process. In the following, the measured output spectrum of the ADC will be presented under various MS conditions. All these measurements were performed at a sampling rate f_s of 61.6 MHz, using a single-tone input frequency $f_{\rm in}$ of 2.5 MHz. The estimates of the ADC output PSD were computed using the Welch procedure with the data windowed using a Kaiser window with $\beta = 21$ [33].

A CFCS ADC with no MS has the measured output spectrum shown in Fig. 26. The measured SNDR is 64.1 dB and SFDR is 67.5 dB at an OSR $= 4$. On the other hand, a mismatch-shaped CFCS ADC using the swapping sequence $sw_{\rm all} = (-1)^n$ has the output spectrum shown in Fig. 27. The measured SNDR is 67.4 dB and SFDR is 76 dB at an OSR $= 4$. This demonstrates

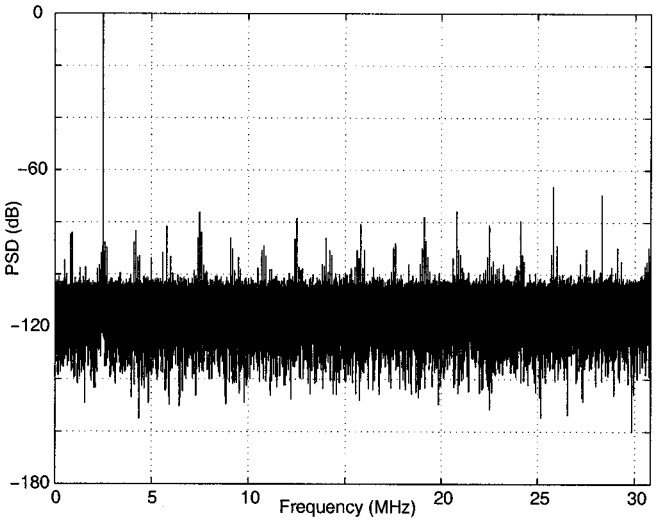

Fig. 27. Mismatch shaped CFCS ADC using $sw_{\rm all} = (-1)^n$: SNDR $= 67.4$ dB, SFDR $= 76$ dB, $f_s = 61.6$ MHz, $f_{\rm in} = 2.5$ MHz, and OSR $= 4$.

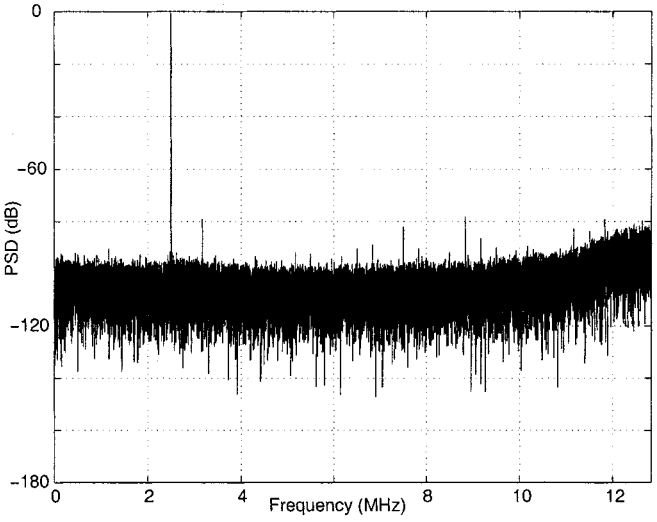

Fig. 28. Mismatch shaping of CFCS ADC using $sw_{\rm all}$ shown in Fig. 20: SNDR $= 64.5$ dB, $f_s = 25.7$ MHz, $f_{\rm in} = 2.5$ MHz, and OSR $= 4$.

an SNDR improvement of 3.3 dB and an SFDR improvement of 8.5 dB. As expected, the second and fourth harmonics have been modulated to half the sampling frequency and the SNDR becomes thermal-noise dominated. The dominant inband harmonic is now the third harmonic, which is caused mainly by signal-dependent charge injection in the sampling circuits and is unaffected by MS, as expected.

Fig. 28 shows the output spectrum at $f_s = 25.7$ MHz for the ADC with MS using a noise-shaped sequence $sw_{\rm all}$ with a spectrum shown in Fig. 20. This measurement was performed at a lower sampling rate due to digital noise feedthrough in the test setup. The measured SNDR and SFDR are 64.5 and 78 dB, respectively.

Figs. 29 and 30 show the INL of the converter without and with MS, respectively. Figs. 31 and 32 show the DNL without and with MS. The INL and DNL plots are obtained using the procedure in [34] from the measured data after it has been filtered digitally to remove the out-of-band signals. MS is applied using the sequence $sw_{\rm all} = (-1)^n$.

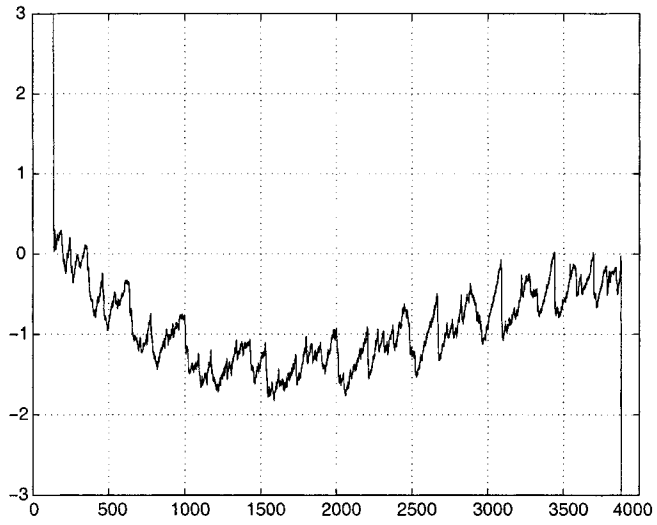

Fig. 29. CFCS INL plot: $f_s = 61.6$ MHz, $f_{\rm in} = 2.5$ MHz, and OSR $= 4$.

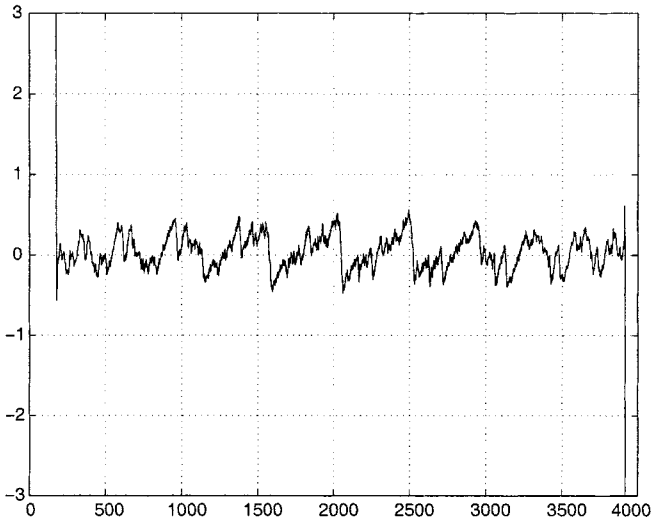

Fig. 30. INL of mismatch shaped CFCS with $sw_{\rm all} = (-1)^n$, $f_s = 61.6$ MHz, $f_{\rm in} = 2.5$ MHz, and OSR $= 4$.

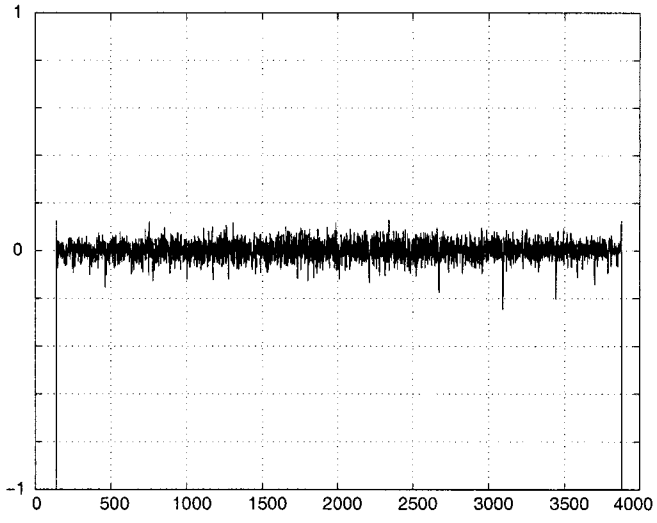

Fig. 31. CFCS DNL plot: $f_s = 61.6$ MHz, $f_{\rm in} = 2.5$ MHz, and OSR $= 4$.

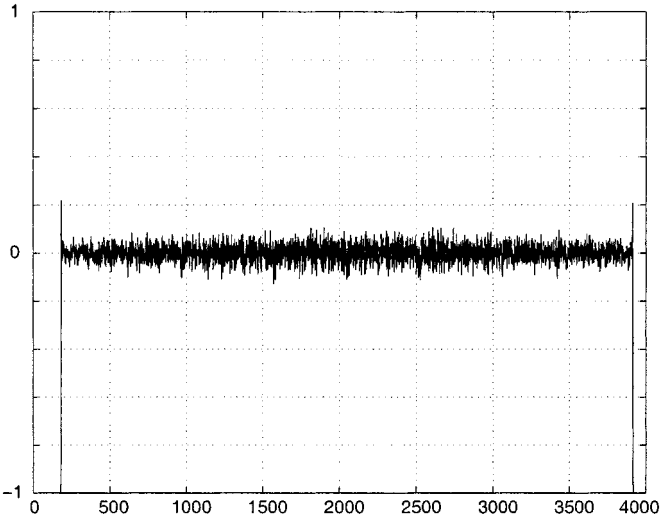

Fig. 32. DNL of mismatch shaped CFCS with $sw_{\rm all} = (-1)^n$, $f_s = 61.6$ MHz, $f_{\rm in} = 2.5$ MHz, and OSR $= 4$.

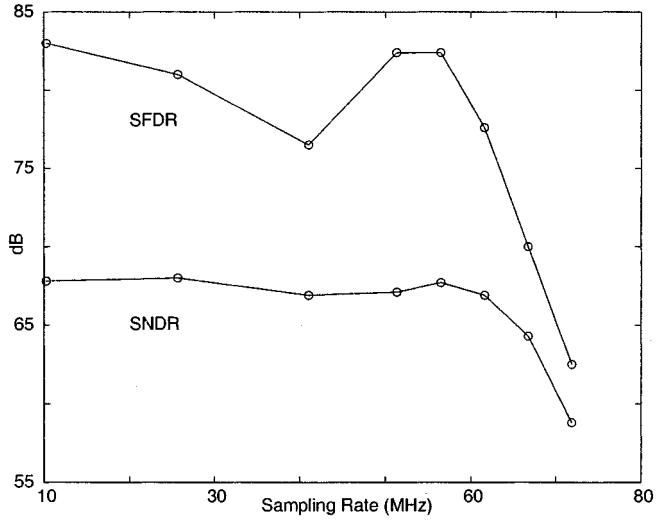

Fig. 33. SNDR and SFDR of a mismatch-shaped converter versus sampling rate ($f_{\rm in} = 0.475$ MHz).

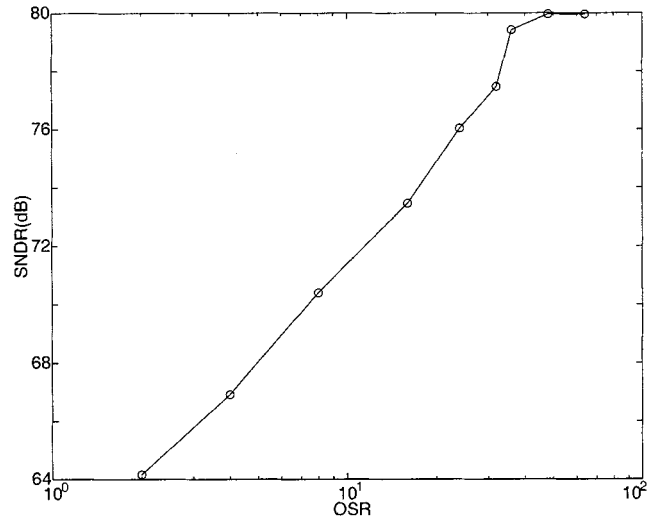

Fig. 34. SNDR of a mismatch shaped converter versus the OSR ($f_s = 61.6$ MHz and $f_{\rm in} = 0.475$ MHz).

TABLE II
SUMMARY OF THE MEASURED PERFORMANCE

Process	0.35um CMOS	
Supply Voltage	3.4V	
Differential Input Range	1.4Vpp	
Resolution (OSR=4)	12bits	
Sampling Rate	61Msample/s	
SNDR (w/o and with MS)	64.1dB	67.5dB
SFDR (w/o and with MS)	67.4dB	76dB
INL (w/o and with MS)	+0.3/-1.8 LSB	+0.6/-0.4 LSB
DNL (w/o and with MS)	+0.12/-0.25 LSB	+0.12/-0.12 LSB
Analog Power Dissipation	435 mW	
Digital Power Dissipation	165 mW	

Fig. 33 plots the SNDR and SFDR as a function of the sampling rate for a mismatch-shaped converter. The converter has a SNDR of at least 67 dB up to a sampling rate of 61 MHz. Beyond this frequency, the performance becomes affected by distortion due to incomplete opamp settling, and the SNDR degrades.

Fig. 34 plots the SNDR as a function of the oversampling ratio. The SNDR improves by 3 dB for every doubling of the OSR, as would be expected from a thermal noise limited converter. The SNDR does not exceed 80 dB, however, as the converter performance becomes dominated by the inband distortion. Table II summarizes the measured performance of the ADC. The digital power consumption includes the power used by the comparators, the digital error correction logic, the output drivers, and the distributed clock phase generator.

VII. CONCLUSION

This paper presented mismatch-shaping techniques to improve the linearity of oversampled pipeline data converters. The techniques do not rely on calibration, but rather they improve the linearity by modulating the distortion energy out of the signal band. This is accomplished without any knowledge of the specifics of the converter nonlinearity, except for the overall structure of the nonlinearity which is constrained to be an even function. The 1-bit/stage CFCS pipeline converter offers the basic building block with the desired nonlinearity structure, and is used to implement mismatch shaping using simple circuit realizations.

ACKNOWLEDGMENT

The authors would like to thank P. Ferguson, T. Barber, and K. Bacrania for significant help throughout the course of this project. They also thank A. Karanicolas, X. Haurie, L. Singer, D. Kelly, S. Ho, J. Lloyd, C. McDonald, J. Lutsky, B. Brandt, P. Holloway, K. Gulati, D. McMahill, C. Sodini, R. Schreier, D. Wu, S. Dacy, M. Spaeth, and M. Peng for helpful comments and suggestions.

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