A 300-MHz BiCMOS Serial Data Transceiver

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Abstract— **A BiCMOS circuit for serial data communication is presented. The chip has phase-locked loops for transmit frequency synthesis and receive clock recovery, serial-to-parallel and parallel-to-serial converters, and encode and decode functions. Since this is a mixed-analog/digital design, and the transmitter and receiver operate asynchronously, many techniques are used to decrease noise coupling. A 1.2 μm BiCMOS process allows operation at speeds of 300 MHz along with this high level of system integration, and the chip consumes less than 1 W from a single 5 V supply.**

I. Introduction

COMPUTER networking services such as electronic mail, network file sharing, diskless nodes, distributed computing, and audio and video data all create demand for more network bandwidth. In addition, nearly every other aspect of computing performance grows exponentially, and thus bandwidth must increase simply to maintain system balance.

Serial data communication circuits interface an analog communication channel to a digital system. System integration requirements lead to the desirability of integrating transmit and receive circuits onto a single die along with some digital circuitry. This application requires a high-performance mixed-analog/digital integrated circuit.

BiCMOS processing technology allows fabrication of high-performance CMOS and bipolar transistors on the same die. BiCMOS technology is a good candidate for serial data communication because this mixed-analog/digital application demands both high-frequency operation and a high level of integration. The ability to combine dense CMOS logic with high-performance bipolar transistor circuits allows many analog and digital operations to be performed on a single die without violating area or power constraints.

This paper presents 300 MHz circuits for serial data communication [1]. A single die fabricated in a 1.2 μm BiCMOS process contains two PLL's—one for transmit frequency synthesis and one for receive clock recovery. The chip also contains encode/decode and serial-to-parallel and parallel-to-serial conversion circuits that allow a 30 MHz parallel digital interface. In addition, a self-test circuit can generate and detect $2^7 - 1$ pseudorandom data.

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Previous PLL's for serial data communication have reported lower communication speeds [2]–[4] or a lower level of system integration [5], [6]. This work demonstrates a circuit with both a high data rate and a high level of system integration. In addition, the transmit and receive sections of the chip operate asynchronously. While this has generally been avoided in the past due to crosstalk and injection locking concerns, problems are avoided through careful circuit design, layout, packaging, and PC board techniques discussed later. Moreover, we exploit the transmit clock to set the reference for the receive PLL to avoid frequency acquisition problems [7].

Section II describes the architecture of the chip and examines a master/slave dual phase-locked loop architecture. The circuit design of some of the phase-locked loop components, the design methodology used for the digital circuits, and the design of the parallel-to-serial converter are examined in Section III. Noise considerations are addressed in Section IV, and experimental results are presented in Section V.

II. System Architecture

A block diagram of the chip is shown in Fig. 1. The transmitter (top) has a 10-b-wide, 30 MHz, CMOS-level interface. Data are encoded by a nonreturn to zero (NRZ) to nonreturn to zero invert on ones (NRZI) encoder. The encoded data are then serialized by a parallel-to-serial converter and are transmitted using differential-ECL levels. A frequency synthesis PLL uses a phase-frequency detector [8], a divide-by-ten prescaler, and a voltage-controlled oscillator (VCO) to generate the 300 MHz transmit clock from a 30 MHz frequency reference.

The receiver (bottom) receives differential 300 Mb/s data at ECL levels, recovers a clock, and regenerates the data. The data are parallelized by a serial-to-parallel converter and are decoded by an NRZI-to-NRZ decoder. Output is 10-b-wide data at CMOS levels, along with a 30 MHz clock. The receive PLL recovers the clock from the serial data stream using a self-aligning phase detector [9], a differential charge pump, and a VCO.

BiCMOS technology is useful for the design as a whole because it allows three different types of circuits to be placed on a single die. The block diagram is shaded to represent the relative portions of CMOS and bipolar transistors found in each block. Lightly shaded blocks, such as the VCO's and the receive phase detector, are mostly bipolar circuits. These circuits operate at the full 300 MHz clock rate, and thus maximum speed operation is desired, and a large power budget is warranted.

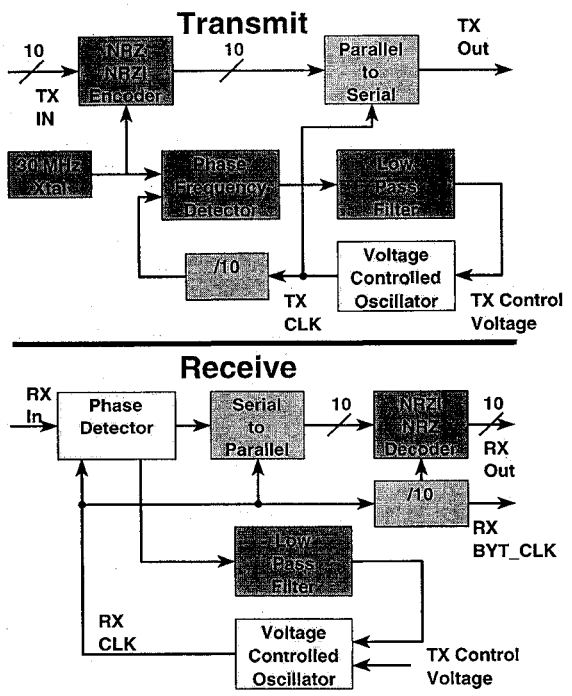

Fig. 1. System block diagram.

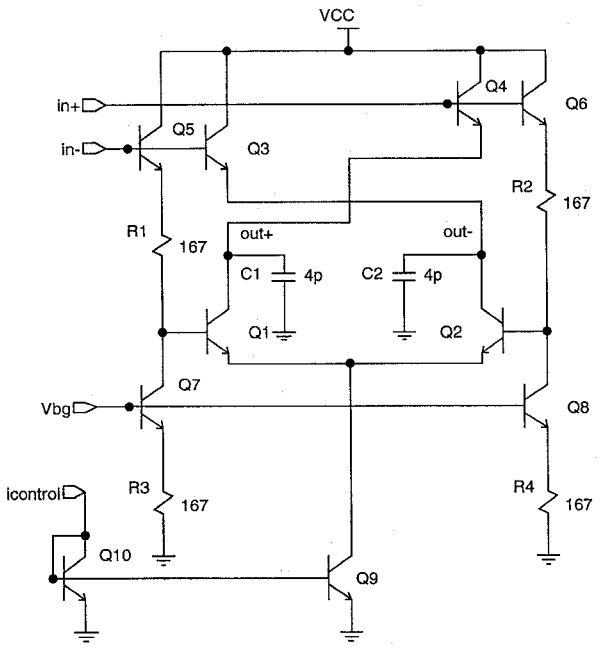

Fig. 2. Voltage-controlled oscillator schematic diagram.

Dark shaded blocks represent circuits where mostly CMOS transistors are used. These circuits operate on 10-b-wide data with a 30 MHz clock. This clock frequency is well within the range of standard CMOS logic. Area, power, and design effort are saved through the use of traditional CMOS logic.

Blocks shaded a medium gray represent circuits where a mix of bipolar and CMOS transistors are used. These blocks share the characteristic that they have both serial and parallel operations, and thus have parts operating at both 30 and 300 MHz. It is in these blocks that BiCMOS technology allows the largest gain in design freedom.

Master/Slave Dual-Loop Architecture: Phase-locked loops with narrow loop bandwidths and multiplying phase detectors have problems with harmonic lock or failure to lock when the input frequency differs significantly from the VCO center frequency [8]. Timing recovery demands narrow loop bandwidth and prohibits the use of phase-frequency detectors due to missing transitions [8]. In the past, this problem has been solved with dual-phase detector loops [10], [3], [4] and complex sequential phase detectors [11].

This circuit uses a master/slave dual-loop configuration where the transmit frequency reference sets the center frequency of the receive loop [12]. The transmit frequency synthesis loop (top) generates the transmit clock from a frequency reference. The receive loop (bottom) uses the transmit loop control voltage as a coarse adjustment to its VCO. This coarse control input to the receive loop is shown in Fig. 1 as the connection of the transmit control voltage to the receive VCO. Feedback for the receive loop is through a fine adjust input on the receive VCO. Since the transmit frequency reference matches the incoming data rate to within crystal tolerances, the center frequency of the receive loop is within the VCO mismatch of the input data rate.

III. Circuit Design

A. Voltage-Controlled Oscillator

The voltage-controlled oscillators used in the transmit and receive circuits are relaxation oscillators [13], [14] consisting of a charging circuits and latches. The charging circuit is shown in Fig. 2. Assuming that in+ is high and in− is low on the charging circuit, $C1$ is held high through $Q4$, and $C2$ is ramped down at a rate of $IC9/C2$ by $Q2$. A differential ECL latch, shown in Fig. 3, waits for the voltage on $C2$ to drop below vtrig and then flips the voltage on in+ and in− so that $C2$ is quickly pulled high and $C1$ is ramped down. The latch then waits for the voltage on $C1$ to drop below vtrig. Since $C1$ and $C2$ are on chip, the circuit uses no external timing elements. In addition, these capacitors are to ground, thus eliminating problems caused by parasitic capacitance to ground in circuits requiring floating capacitors. Temperature and supply stability are achieved through the use of an on-chip bandgap reference.

B. Phase Detector

The receive phase detector, shown in Fig. 4, is a self-aligning type detector [9] and is composed of two ECL D-flip/flops and two ECL exclusive OR gates. This phase detector output drives a differential charge pump and loop filter before being fed back to the VCO. The charge pump is shown in Fig. 5. Two current switches composed of $Q4$–9 steer current to or away from on-chip capacitors $C1$ and $C2$. An external series-RC loop filter is connected across $C1$ and $C2$. A common mode feedback circuit composed of $M1$–6 keeps the common mode of out+ and out− equal to vref by adjusting the currents through $M7$ and $M8$ to equal the currents through $Q5$ and $Q8$.

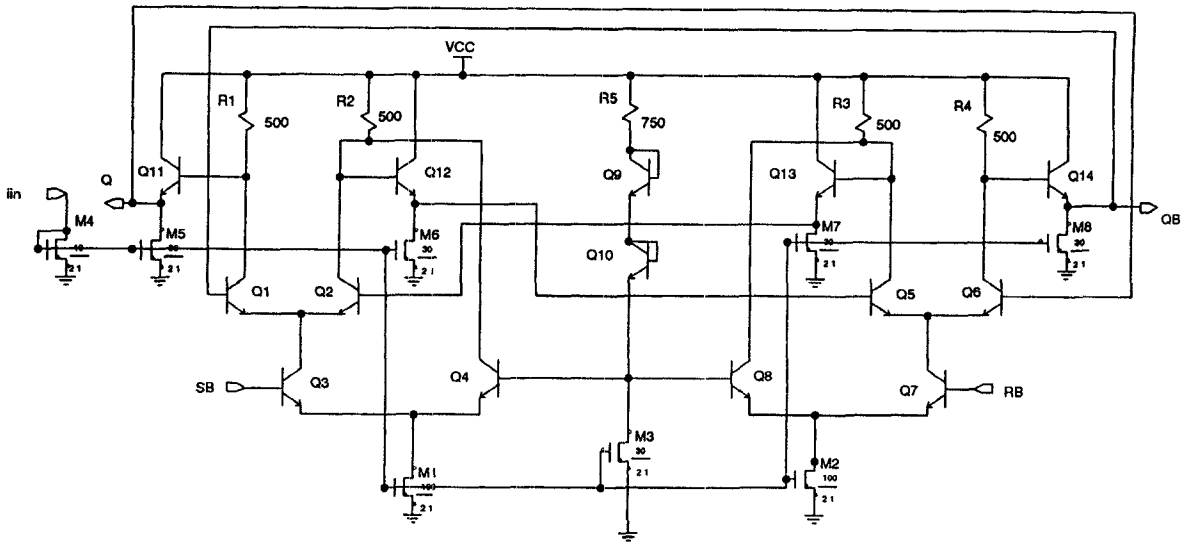

Fig. 3. Differential-ECL latch schematic diagram.

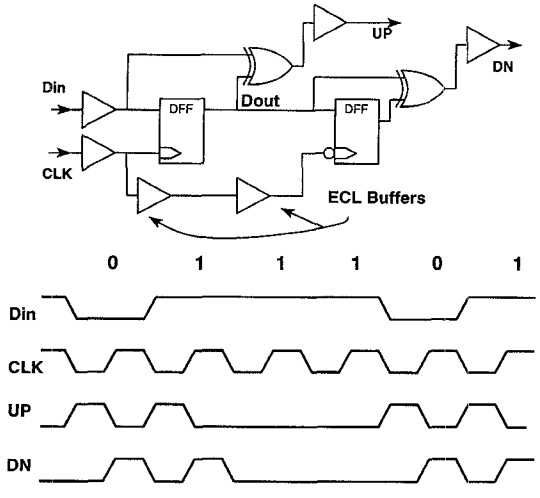

Fig. 4. Receive phase detector.

To examine the operation of the CMFB circuit, assume that the voltages on out+ and out− drift higher than the voltages at the gates of $M3$ and $M6$. The current through $M1$ amd $M4$ will increase, and the current through $M3$ and $M6$ will decrease. $M5$ sets the current through $M7$ and $M8$ to the sum of the currents through $M3$ and $M6$. Since both of these currents decrease, the currents through $M7$ and $M8$ decrease to match the currents through $Q5$ and $Q8$. This decreases the voltages on out+ and out−.

C. Digital Design Methodology

Many blocks in the system perform digital logic functions. Some of them operate on serial data and are clocked at the full data rate, while others operate on parallel data and are clocked at much lower data rates. The design flexibility of BiCMOS allows these blocks to be implemented in very different logic styles. Three styles of logic are used in various portions of the design.

For the highest speed circuit blocks operating at the full bit-rate clock (300 MHz), differential-ECL circuits with 1 mA tail currents and 0.5 V swings are used. This logic style is capable of producing faster toggle rates and shorter propagation delays than the other logic forms used in the design. Unfortunately, this logic style also has high static power dissipation and occupies much more area per gate than any other logic style used in this design. Use of differential ECL is therefore restricted to only speed-critical circuit elements.

Some digital logic operates with a one-half bit-rate clock (150 MHz). In these cases, dynamic-CMOS flip-flops are used with less than three stages of combinational logic between flip-flops. The dynamic flip-flop, shown as the shifter cell in Fig. 10, has only eight transistors, and is thus very area and power efficient. The low parasitic capacitances associated with this flip-flop and a small number of logic stages allow high-frequency operation.

Parallel blocks clocked with the byte clock (30 MHz) are implemented in standard static-CMOS logic. This logic form combines low power, low area, robustness, and design ease. Standard logic synthesis and automated layout tools can be used for these blocks since this clock rate is in the standard operating range for CMOS logic.

Due to design complexity, area, and power considerations, whenever there is a choice of logic styles that can be used, the slowest possible style is chosen. This can even be the case when it takes many more gates to implement a function in the slower style. For instance, encoder and decoder functions are frequently implemented using high-speed serial circuits; but operations of this type can often be converted into parallel operations [15]. The parallel operation may require many more gates, but it operates at slower speed so that it can be implemented in standard CMOS logic.

To demonstrate the advantages of a parallel implementation, consider the parallel and serial implementations of the NRZI-to-NRZ converter shown in Figs. 6 and 7. The serial

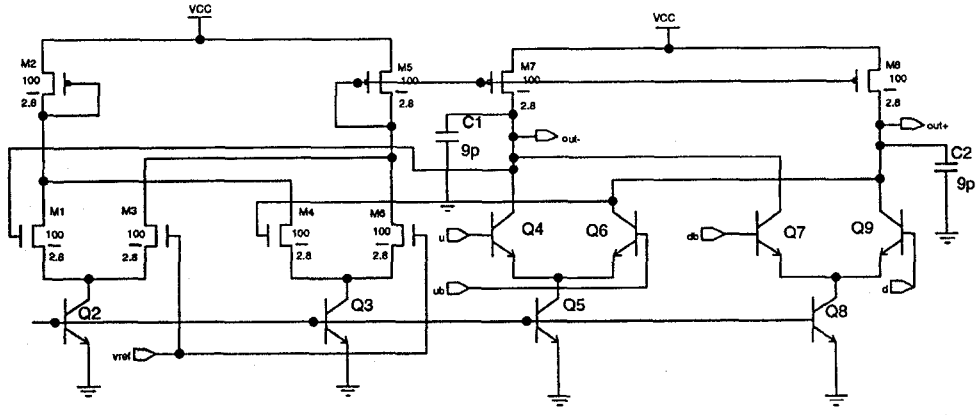

Fig. 5. Charge pump schematic diagram.

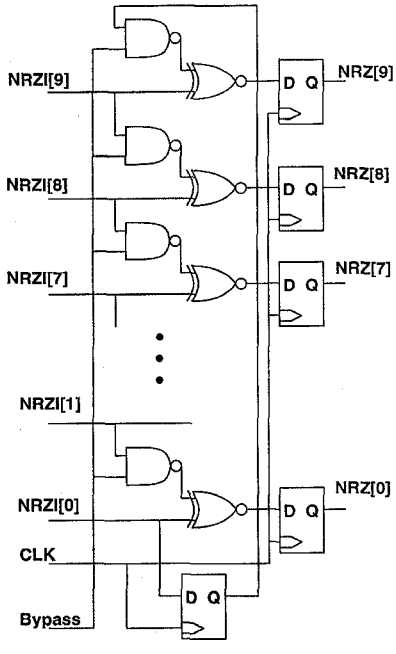

Fig. 6. NRZI-to-NRZ parallel implementation.

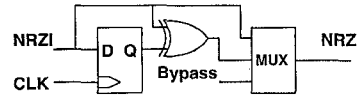

Fig. 7. NRZI-to-NRZ serial implementation.

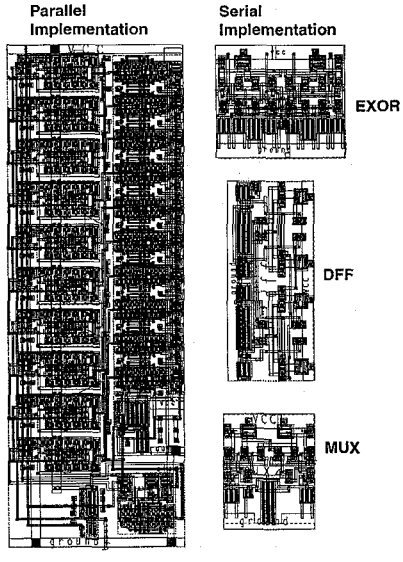

Fig. 8. NRZI-to-NRZ serial and parallel implementation layouts.

implementation operates on bit-wide data with a bit-rate clock. The parallel implementation operates on 10-b-wide data with a byte-rate clock. Both implementations include a multiplexer to allow bypassing of the converter.

The serial implementation consists of just one EXOR gate, one two-to-one MUX, and one *D* flip-flop. Together, these gates dissipate 43 mW of static power. The parallel implementation uses 10 NAND gates, 10 EXOR gates, and 11 *D* flip-flops. There is no static power dissipated by this logic, and simulation shows the dynamic power dissipated by this circuit to be just 1 mW.

Fig. 8 demonstrates that the areas of the two implementations are comparable. This example clearly shows the advantage of CMOS logic—40 gates of CMOS logic consumes 1/40 the power and about the same area as four gates of ECL logic. In addition, the serial implementation requires careful circuit design and layout, while the design and layout of the parallel implementation can be automated with CAD tools.

D. Parallel-to-Serial Converter

A good example of application of the methodology presented above is the parallel-to-serial converter. A block diagram of this converter is shown in Fig. 9. 10-b-wide data are converted into even and odd data streams by two 5 : 1 CMOS multiplexors clocked from a 150 MHz, or half data rate, clock. These two data streams are then converted to ECL levels and latched by two differential-ECL flip-flops. The odd data path is then delayed an extra half clock cycle by an ECL latch clocked on the opposite phase from the flip-flops. An ECL 2 : 1 multiplexor generates the serial output stream by selecting the data stream that is stable during each phase of the clock; since the even stream changes after a rising edge and the odd stream changes after a falling edge on a half data

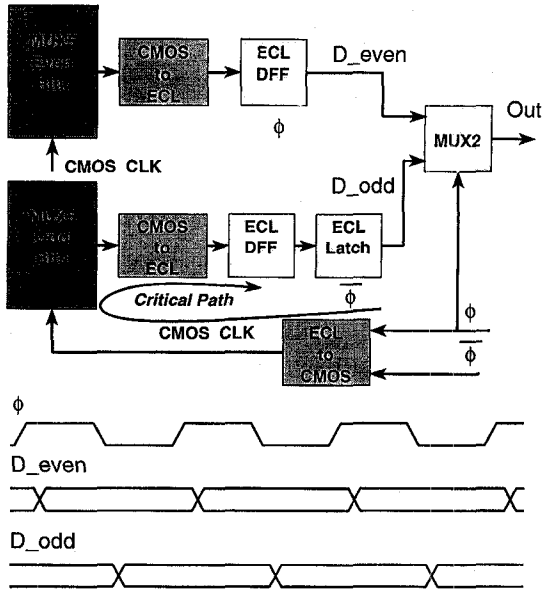

Fig. 9. Parallel-to-serial converter block diagram. The shading represents relative portions of bipolar versus CMOS transistors. Darker blocks have more CMOS transistors, while lighter blocks are predominately bipolar.

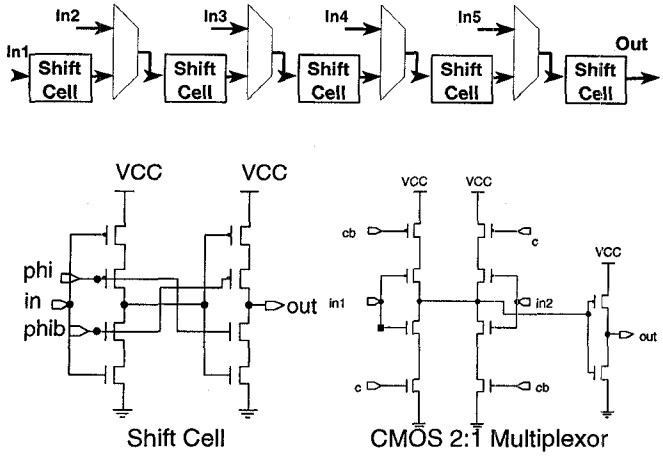

Fig. 10. CMOS 5 : 1 multiplexor.

rate clock, the odd stream is selected when the clock is low, and the even stream is selected when the clock is high.

The constraints on the clocking of this circuit are quite stringent. The ECL clock must have a 50% duty cycle, as any error in duty cycle will produce different length even and odd bits or *pulse pairing*. The logic diagram at the bottom of Fig. 9 shows the signals at the input of the ECL 2 : 1 multiplexor. If the clock does not have a 50% duty cycle, bits from the even or odd data stream will last longer than bits from the other stream. This difference results in transmit jitter. A 50% duty cycle differential-ECL clock is generaed by dividing a full data rate clock by two.

The CMOS 5 : 1 multiplexors require two low-skew half data rate differential clock phases. BiCMOS allows the generation of these low-skew differential clocks because the two phases of the differential-ECL clock have very low skew. These ECL clock phases are sent through two ECL-to-CMOS converters (Fig. 11, top) to generate the required CMOS clocks. The principal cause of skew between these clock phases is mismatch between the ECL-to-CMOS converters. This is better than the normal CMOS case where two clock phases are generated from a single phase CMOS clock and skew results from the extra signal inversion in the path of one of the clock phases.

The critical speed path in this design is the part of the circuit where ECL clock pulses go through an ECL-to-CMOS converter and clock the 5 : 1 multiplexors. The output from these multiplexors then goes through a CMOS-to-ECL converter and is latched by an ECL flip-flop. The time to propagate through this path must be less than the half data rate clock period. This means that the delay through these level converters and through the 5 : 1 multiplexors must be minimized.

A schematic diagram of the 5 : 1 multiplexor is shown in Fig. 10. The multiplexor is composed of five cascaded shift register cells with four 2 : 1 multiplexors allowing selection of the shifted data or the parallel input data. The 2 : 1 multiplexor and dynamic-CMOS shifter cell schematic diagrams are shown at the bottom of this figure. This circuit design style allows compact layout and high-speed operation. This is important because these circuits operate at the half data rate clock.

A schematic diagram of the ECL-to-CMOS converter is shown at the top of Fig. 11. To increase the conversion speed of this conventional converter, the input is driven by a double-swing ECL buffer. This produces a 33% speed increase compared to the same circuit with a normal ECL input.

The CMOS-to-ECL converter is shown in Fig. 11 (bottom). The CMOS input is attenuated by nMOS inverter $M1$ and $M2$. The gain from in1 to X is set so that the ECL buffer sees an ECL-logic swing at X. The low gain of the inverter allows fast circuit operation and minimizes switching glitches in the ECL signals generated by CMOS voltage swings.

The dc voltage at X is set by $M3$ and vbias. A replica bias circuit (right), consisting of $M8$–$M14$, $Q5$ –$Q7$, and $R3$–$R4$, generates vbias. This bias circuit adjusts vbias so that the voltage at Y equals vmid. Since the replica bias and converter circuits are identical, X is also at vmid when in1 is at vmid.

The bias for the tail currents in this cell is input as a 100 μA current at iin and is generated by an on-chip bandgap reference. The transmission of this reference as a current decreases noise generated by differences in ground potential between the reference generator and the circuit using the reference.

The 2 : 1 multiplexor and ECL latches are differential-ECL designs. A tail current of 1 mA and load resistance of 500 Ω produce a 0.5 V logic swing. These circuits use the same current reference scheme as the CMOS-to-ECL converter.

IV. Noise Considerations

One of the key challenges in this design is noise isolation. This is a mixed-analog/digital design, so digital switching noise can couple into sensitive analog nodes. Furthermore, the transmit and receive PLL's operate asynchronously. The transmitter and receiver must be isolated in such a way that these two PLL's can remain asynchronous.

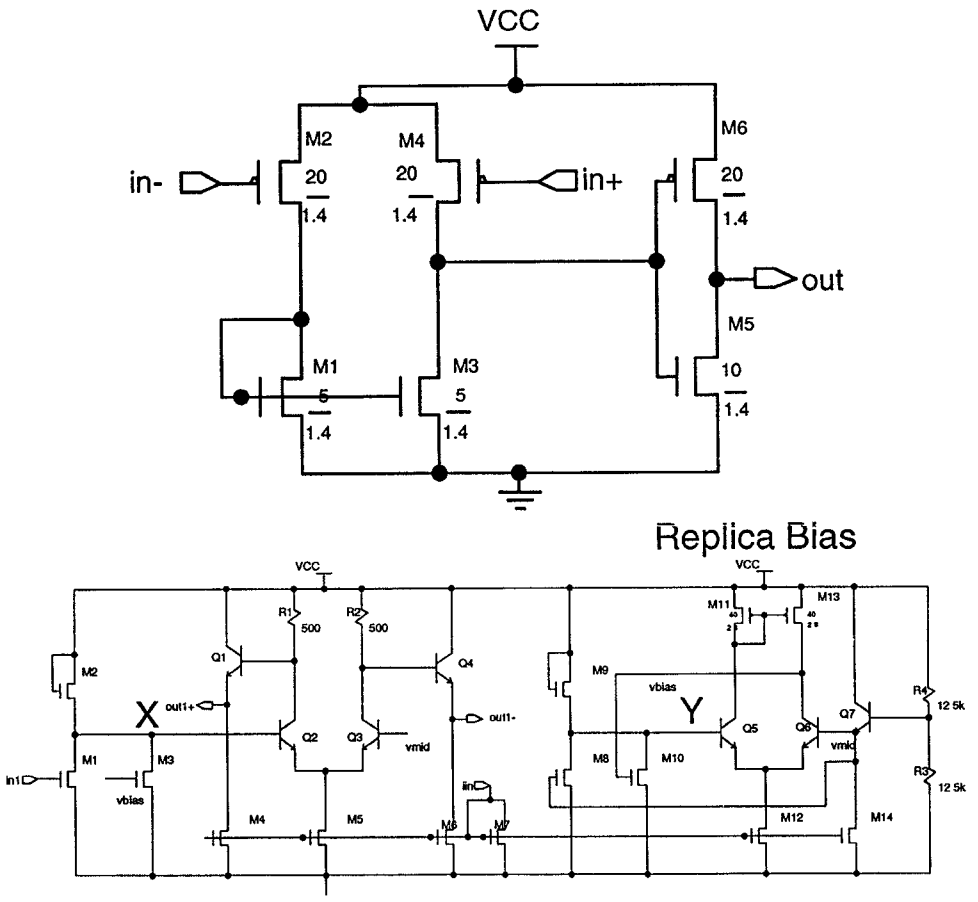

Fig. 11. Level converter schematic diagrams.

TABLE I
EXPERIMENTAL RESULTS

Frequency Range	100–315 MHz
Supply Voltage	5 V
Die Area	28 000 mil^2
Power Consumption at 300 Mb/s	1 W
Host Interface	10 b CMOS
Line Interface	Differential ECL
Transmit Jitter	63 ps rms
Receive Jitter	50 ps rms
Package	64-pin QFP
Process	1.2 μm BiCMOS

Some of the ciruit, layout, packaging, and PC board techniques employed to maintain a quiet noise environment follow.

- Nine separate power supplies are used on the chip. Each of these supplies has its own power and ground pin. On the PC board, these power supplies have separate bypass capacitors and are isolated from each other by ferrite beads.
- Local bias generators are used throughout the design. No reference crosses the transmit/receive boundary, and currents are used instead of voltages to transport references.
- Substrate connections are made only to separate substrate grounds. These grounds carry no power supply current, and separate pins are used for transmit, receive, analog, and digital substrate grounds.
- Slew-rate-limited CMOS output drivers are used. These I/O circuits use a separate power supply.
- Differential circuits are used where possible. Differential control voltages are used in both PLL's, allowing noise to be attenuated by the CMRR of these circuits.
- The chip has 800 pF of on-chip bypass capacitance to supply current demands for switching transients. This capacitance is divided into four approximately equal banks of bypass capacitance for the transmit-digital, transmit-analog, receive-digital, and receive-analog supplies.

V. EXPERIMENTAL RESULTS

The circuit described above was fabricated in a 1.2 μm BiCMOS process and packaged in a low-inductance 64-pin quad flat pack (QFP) package. A die photograph is shown in Fig. 12. The die area is 28 000 mil ^{2} including all the circuits discussed above and the on-chip timing and bypass capacitors. Power dissipation totals about 1 W. Experimental results for this chip are summarized in Table I.

Some of these parts were also packaged in a 68-pin leadless chip carrier (LCC) package. This package is larger than the QFP and has longer bond wires and thus higher inductance. Chips in this package displayed much more jitter than chips in the QFP. In 100 Mb/s operation, recovered clock jitter was 50% higher for the LCC than the QFP. The receiver in the LCC package was unable to lock to incoming 300

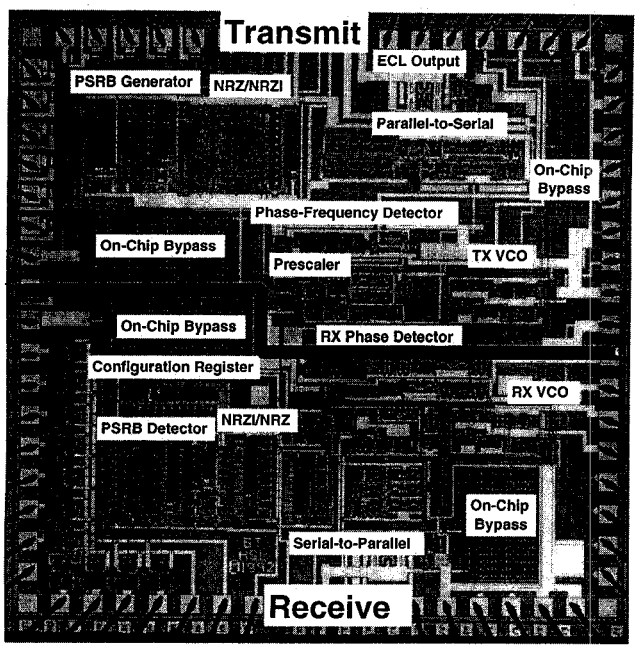

Fig. 12. Die photograph.

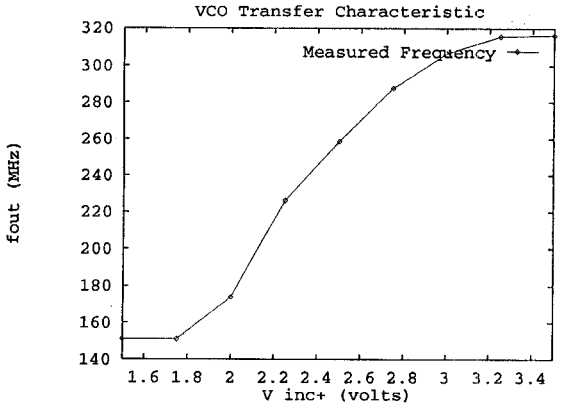

Fig. 13. Measured voltage-controlled oscillator transfer characteristic.

Mb/s data. This shows that in designs where a good noise environment is required, low-inductance packages can be of great value.

The measured VCO transfer characteristic in Fig. 13 shows an operating frequency range of 150–315 MHz. The chip also has a selectable divide-by-two circuit at the output of the VCO so that another frequency range of 75–158 MHz can be selected.

Fig. 14 shows the transition region of the transmitter eye pattern. The data are a 300 Mb/s, 2^7 pseudorandom data stream produced by on-chip self-test circuits. This figure shows transmitter jitter of about 63 ps rms.

Fig. 15 shows clock recovery from a 2^7 pseudorandom input pattern at 300 Mb/s. These data were taken while the transmitter on the same chip was simultaneously generating and transmitting another asynchronous pseudorandom 300 Mb/s data stream. This figure shows the jitter to be 50 ps rms.

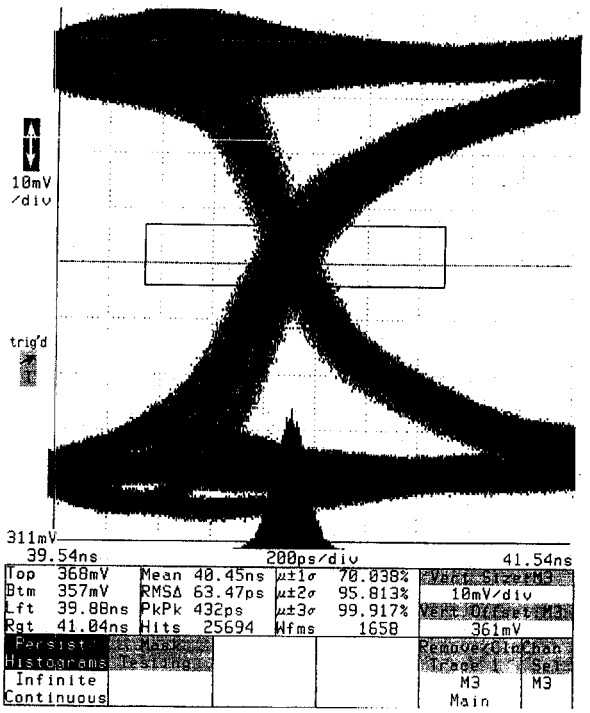

Fig. 14. Transmitter jitter at 300 Mb/s.

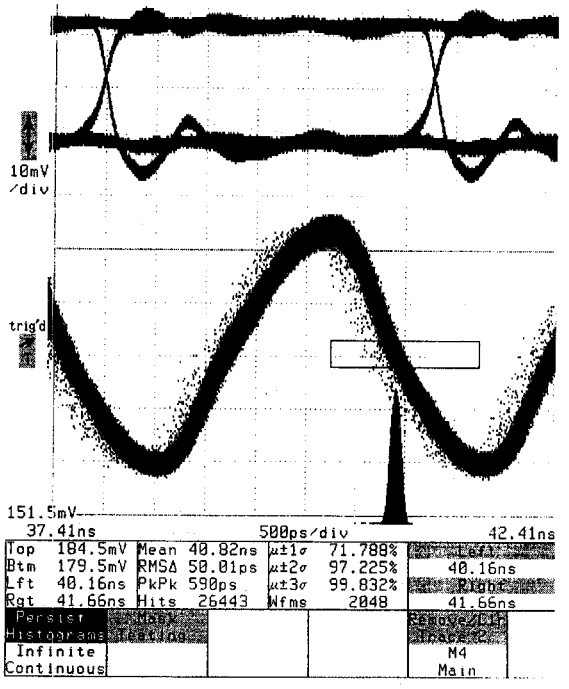

Fig. 15. Receiver jitter at 300 Mb/s.

VI. Conclusion

Table I summarizes measured results from the serial transceiver. No other 300 MHz data communication chip reported to date has a high a level of integration. This combination of analog performance and level of integration clearly demonstrates the advantages of BiCMOS technology for serial data communication applications.

Digital functions on the chip are implemented with a combination of three logic styles: differential ECL, dynamic CMOS, and static CMOS. This combination of logic results in logic that is both faster than CMOS and lower in power and area than ECL. Logic functions often implemented with fast serial circuits are implemented with slower parallel circuits, resulting in significant savings in power and design effort.

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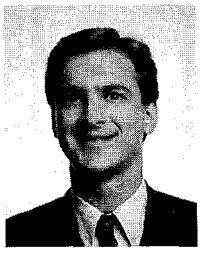

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