A 12–b 600 ks/s Digitally Self-Calibrated Pipelined Algorithmic ADC

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Abstract— **This paper discusses fully digital error correction and self-calibration which correct errors due to capacitor mismatch, charge injection, and comparator offsets in algorithmic A/D converters. The calibration is performed without any additional analog circuitry, and the conversion does not need extra clock cycles. This technique can be applied to algorithmic converter configurations including pipelined, cyclic, or pipelined cyclic configurations. To demonstrate the concept, an experimental 2-stage pipelined cyclic A/D converter is implemented in a standard 1.6-μm CMOS process. The ADC operates at 600 ks/s using 45 mW of power at $\pm$2.5 V supplies. The active die area excluding the external logic circuit is 1 mm^2. Maximum DNL of $\pm$0.6 LSB and INL of $\pm$1 LSB at a 12-b resolution have been achieved.**

I. Introduction

THIS paper describes a pipelined algorithmic A/D converter which employs digital self-calibration and digital error correction. In an algorithmic A/D converter, a variety of errors including capacitor mismatch, charge injection, and comparator offsets result in differential nonlinearity (DNL) and integral nonlinearity (INL). Previous approaches of correcting capacitor mismatch in algorithmic converters include the ratio independent [1], reference refreshing [2], and error averaging [3] approaches, which require additional clock cycles during the normal conversion, making the conversion slower. They also require two operational amplifiers per stage doubling the power and complexity. The analog calibration [4]–[6] requires a calibration DAC for the correction of each stage increasing the complexity and capacitive loading on op amps. In conventional algorithmic converters, the charge injection is reduced by the use of small sampling switch and differential sampling. The small sampling switch may compromise conversion speed in this case. Comparator offsets have been removed by standard offset cancellation requiring power, complexity and resulting in slow response time.

In this paper, an approach is described that employs a nominal radix 2, 1.5 b/stage conversion algorithm. A 1.5 b/stage converter with capacitor ratio error cancellation has been previously reported [7], which is applicable only to a nonpipelined single stage cyclic converter, and hence is slow. Furthermore, it requires a separate S/H amplifier, essentially doubling power and complexity. Other converters using the 1.5 b/stage algorithm were reported recently [8], [9]. However, these converters lacked calibration [8] or must be calibrated using a highly accurate external D/A converter [9].

A fully digital calibration was previously employed in a two-step flash ADC [10]. Although effective for calibration of a single stage, this technique suffers from DNL errors due to the accumulation of quantization errors if more than one stage is calibrated. The removal of such DNL errors requires considerable increase of complexity in the calibration algorithm and circuitry.

The technique discussed in this paper can be applied to cyclic or pipelined algorithmic converters, does not require extra clock cycles during the conversion, and no additional analog circuitry is needed. The analog circuit is simple, using one operational amplifier and two latches per stage. As will be shown in Section III, the 1.5 b/stage algorithm makes simple self-calibration possible in the digital domain. The combination of digital error correction and calibration removes any error due to capacitor mismatch, charge injection, and comparator errors, including offset and noise. The gain of each stage is precisely calibrated, so that multistage calibration does not introduce the DNL as in [10], and the overall converter has a precise full-scale of $\pm V_{REF}$. Since the comparator decision error up to 1/4 full scale is corrected, the comparator can be strobed before the op amp has fully settled. Therefore the comparator decision delay does not cut into the conversion time. The high tolerance to comparator errors also permits the use of a simple latch as a comparator.

The digital calibration converts the raw digital outputs into correct codes. In effect, it can only reassign correct digital codes to the appropriate analog input voltage ranges, but cannot create new decision levels. Therefore, the uncalibrated converter must provide all the necessary decision levels. In conventional algorithmic converters, this condition cannot be satisfied if capacitor mismatch, charge injection, or comparator offset are present. It can be shown that the 1.5 b/stage algorithm guarantees this condition and makes a simple digital calibration possible as explained in the following sections.

II. 1 b/Stage A/D Converter

Most conventional 1 b/stage algorithmic or pipeline A/D converters employ a nominal radix-2 algorithm [1]–[4]. A simplified block diagram of a single stage of such a converter is shown in Fig. 1. Each stage consists of two nominally equal capacitors C_1 and C_2, an operational amplifier, and a comparator. During the sampling phase shown in Fig. 1(a), the input voltage $V_{in}(i)$ presented to stage i is sampled on C_1 and C_2. At this time, the comparator compares $V_{in}(i)$ with

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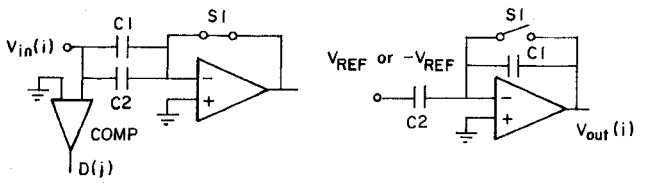


(a) (b)

Fig. 1. Radix-2 1-b/stage algorithmic A/D converter: (a) sampling phase, (b) multiply-by-2 (M × 2) phase.

ground (GND), producing the digital output $D(i)$:

$$D(i) = 1 \text{ if } V_{\text{in}}(i) > 0 \text{ and}$$
$$D(i) = -1 \text{ if } V_{\text{in}}(i) < 0. \quad (1)$$

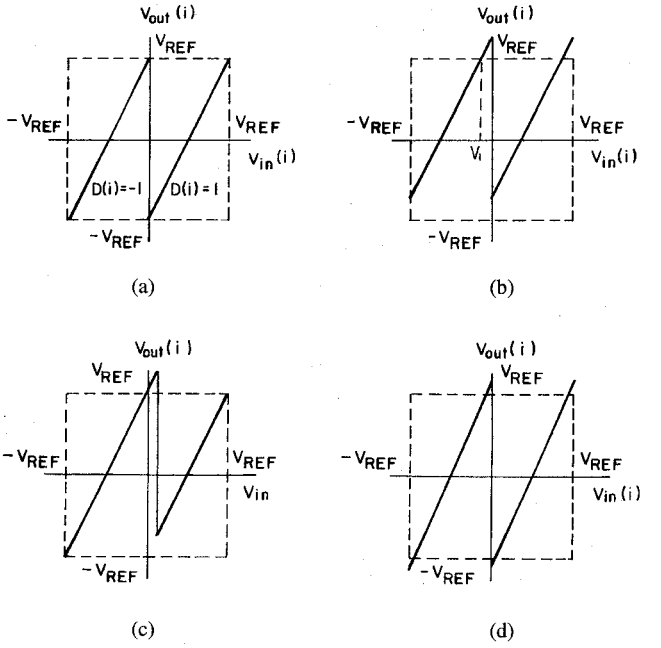
During the multiply-by-2 (M × 2) phase shown in Fig. 1(b), C_1 is connected to the output of the op amp, while C_2 is connected to V_{REF} or $-V_{\text{REF}}$ depending on the digital output code $D(i)$. If charge injection is ignored and $C_1 = C_2$, the output voltage $V_{\text{out}}(i)$ can be written

$$V_{\text{out}}(i) = 2V_{\text{in}}(i) - D(i)V_{\text{REF}}. \quad (2)$$

This output voltage is then passed to the next stage $i+1$, and the same operation continues. The output voltage $V_{\text{out}}(i)$ of each stage is referred to as the residue, the plot of which is shown in Fig. 2. Fig. 2(a) indicates an ideal residue plot where the output voltage is expressed in (2). In Figs. 2(b) through (d), the effects of charge injection, comparator offset, and capacitor mismatch are indicated. Referring to Fig. 2(b), charge injection from the sampling switch $S1$ results in a vertical shift of the transfer characteristic. As a result, near the center of the input range, the output exceeds V_{REF} for the input range $V_1 < V_{\text{in}} < 0$. Assuming the subsequent stages are ideal, the output codes of the subsequent stages remain all 1's for $V_1 < V_{\text{in}} < 0$. This results in "missing decision levels" because a wide range ($V_1 < V_{\text{in}} < 0$) of input corresponds to a single digital output code. As explained previously, missing decision levels cannot be corrected by digital calibration only. Similarly, comparator offsets and capacitor mismatch can cause the residue output to exceed V_{REF} or $-V_{\text{REF}}$, consequently missing decision levels. Therefore, in nominal radix-2 converters, in general, fully digital calibration is not possible. A non-radix-2 conversion algorithm has been suggested to prevent missing decision levels so that fully digital calibration is possible [11]. This paper presents an alternative approach using a nominal radix-2, 1.5 b/stage algorithm [12]. The technique presented in [11] offers higher calibration accuracy while the calibration outlined in this paper provides a precise full-scale and higher tolerance to comparator offsets, up to ±1/4 V_{REF}, compared to 1.75% of V_{REF} in [11].

III. 1.5 b/Stage A/D Converter

Consider a fully pipelined converter employing the 1.5 b/stage algorithm, one stage of which is shown in Fig. 3. Although a fully differential configuration is preferred in practice, a single-ended version is shown in the figure for simplicity. In the fully differential circuit matching between



(a) (b) (c) (d)

Fig. 2. Residue plot of radix-2 1-b/stage algorithmic ADC: (a) ideal residue, (b) with charge injection, (c) with comparator offset, (d) with capacitor mismatch ($\alpha > 0$).

V_{REF} and $-V_{\text{REF}}$ it is not necessary. During the sampling phase shown in Fig. 3(a), both $C1$ and $C2$ are connected to the input voltage $V_{\text{in}}(i)$ and the op amp is connected in the unity-gain mode. The input voltage to the ith stage $V_{\text{in}}(i)$ is compared with two levels, $V_+(0 < V_+ < V_{\text{REF}}/2)$ and $V_-(-V_{\text{REF}}/2 < V_- < 0)$ neither of which needs to be accurate. For simplicity of discussion, the bit decisions from two comparators are represented by three values $D(i) = 1$, 0, and -1 as follows:

$$D(i) = -1 \text{ if } V_{\text{in}}(i) < -V_-$$
$$D(i) = 0 \text{ if } V_- < V_{\text{in}}(i) < V_+$$
$$D(i) = 1 \text{ if } V_{\text{in}}(i) > V_+. \quad (3)$$

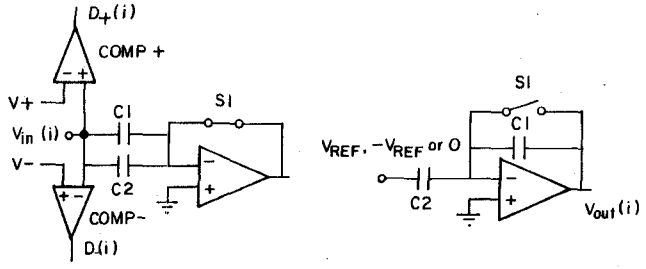
During the M × 2 phase, $C1$ is connected to the output, and $C2$ is connected to V_{REF}, 0, or $-V_{\text{REF}}$ depending on the bit decision made in the first phase, as shown in Fig. 3(b). The output voltage for the ith stage in an ideal case is

$$V_{\text{out}}(i) = 2V_{\text{in}}(i) - D(i)V_{\text{REF}} \quad (4)$$

where

$$D(i) = +1, 0, \text{ or } -1.$$

The ideal residue plot is shown in Fig. 4(a), while the effects of charge injection, comparator offset, and capacitor mismatch are indicated in Figs. 4(b)–(d). Note that the residue output never gets close to $\pm V_{\text{REF}}$ at code transition points. Thus, missing decision levels, which result when the residue output exceeds $\pm V_{\text{REF}}$ at code transition points, are prevented. The digital error correction is inherent in this algorithm, and any comparator error less than $\pm 1/4\ V_{\text{REF}}$ is corrected, The charge injection manifests itself only as overall input referred offset voltage which is easily taken out by the digital calibration as explained in the next section. The capacitor mismatch gives



(a) (b)

Fig. 3. The 1.5 b/stage algorithmic ADC (a) sampling phase, (b) multiply-by-2 (M × 2) phase.

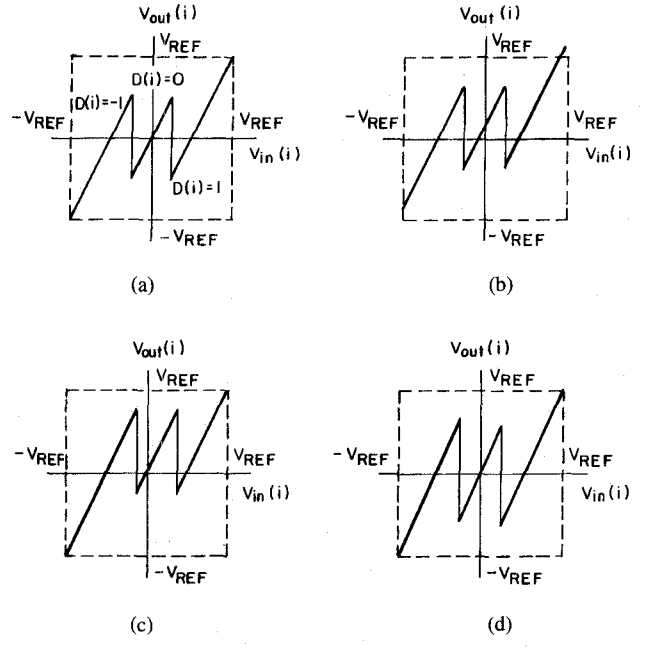


Fig. 4. Residue plot of 1.5 b/stage algorithmic ADC: (a) ideal residue, (b) with charge injection, (c) with comparator offset, (d) with capacitor mismatch ($\alpha > 0$).

rise to DNL and INL and must be corrected by the digital calibration.

IV. Digital Self-Calibration

As discussed in the preceding section, the only error that causes linearity error in a 1.5 b/stage converter is the capacitor mismatch (assuming that the operational amplifier has high enough gain). The ratio mismatch in nominally identical capacitors $C1$ and $C2$ is indicated as α_i where $C_2 = (1 + \alpha_i)C_1$. In this case, the output voltage is

$$V_{\text{out}}(i) = 2(1 + \alpha_i/2)V_{\text{in}}(i) - D(i)(1 + \alpha_i)V_{\text{REF}} \quad (5)$$

Equation (5) is identical to (4) if the mismatch α_i is zero. If an analog correction voltage $-\alpha_i V_{\text{in}}(i) + D(i)\alpha_i V_{\text{REF}}$ is added to $V_{\text{out}}(i)$, an ideal output voltage in (4) is produced. In fully digital calibration, the analog correction voltage can be replaced by a digital value $D[-\alpha_i V_{\text{in}}(i) + D(i)\alpha_i V_{\text{REF}}]$

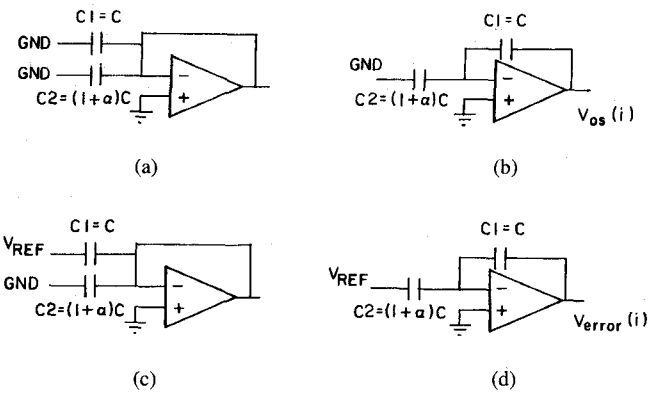


Fig. 5. Calibration cycles (a) offset measurement: sampling phase, (b) offset measurement: M × 2 phase, (c) capacitor mismatch measurement: sampling phase, (d) capacitor mismatch measurement: M × 2 phase.

which is the digitized analog correction voltage. Referred to the input of the first stage, the digital approximation of $V_{\text{in}}(i)$ is $\frac{1}{2^i}[D(i)/2 + D(i+1)/4 + D(i+2)/8 + \cdots]$ while the digital value of $D(i)\alpha_i V_{\text{REF}}$ is $\frac{1}{2^i}D(i)\alpha_i$. Thus, if α_i is known, the error can be canceled by adding a digital correction quantity $\varepsilon(i)$ to the digital output:

$$\begin{aligned}\varepsilon(i) &= D[-\alpha_i V_{\text{in}}(i) + D(i)\alpha_i V_{\text{REF}}] \\ &= -\frac{\alpha_i}{2^i}[D(i)/2 + D(i+1)/4 + D(i+2)/8 + \cdots] \\ &\quad + \frac{\alpha_i}{2^i}D(i) \\ &= \frac{\alpha_i}{2^i}[D(i)/2 - D(i+1)/4 - D(i+2)/8 - \cdots]. \quad (6)\end{aligned}$$

The quantization error in calibration is typically reduced by adding 2 more bits in the pipeline or cyclic conversion. The calibration measurements are averaged many times (typically 256 times) to further reduce quantization and circuit noise. The calibration of other stages is done in the same manner. From (6) and similar equations for other stages, the correction term that corresponds to each bit $D(i)$ is calculated during the initial calibration cycles, and stored in RAM. For a 12-b converter, a 6-byte memory is sufficient if the first 6 stages are calibrated. During the normal conversion, these correction terms are added to the conversion result to calibrate errors in all the stages that are calibrated. It should be noted that the calibration requires only digital additions or subtractions. An adder/subtractor is needed for each stage being calibrated. Therefore, a total of 6 12-b adders are required for a fully pipelined 12-b converter in which the first 6 stages are calibrated. In a fully-pipelined converter, α_i corresponds to the ratio error in each stage. In an N-stage cyclic converter, $\alpha_i = \alpha_{i+N}$ because the same stages are reused. For example, for a 2-stage cyclic converter, $\alpha_1 = \alpha_3 = \alpha_5 = \cdots$ and $\alpha_2 = \alpha_4 = \alpha_6 = \cdots$. The number of adders is reduced by the factor of the number of recirculations in a conversion.

The measurements the α's during the initial calibration period are done as illustrated in Fig. 5. First, 0 V is used as an input to the ith stage, which is digitized by the ith and the following stages as shown in Figs. 5(a) and (b). The result

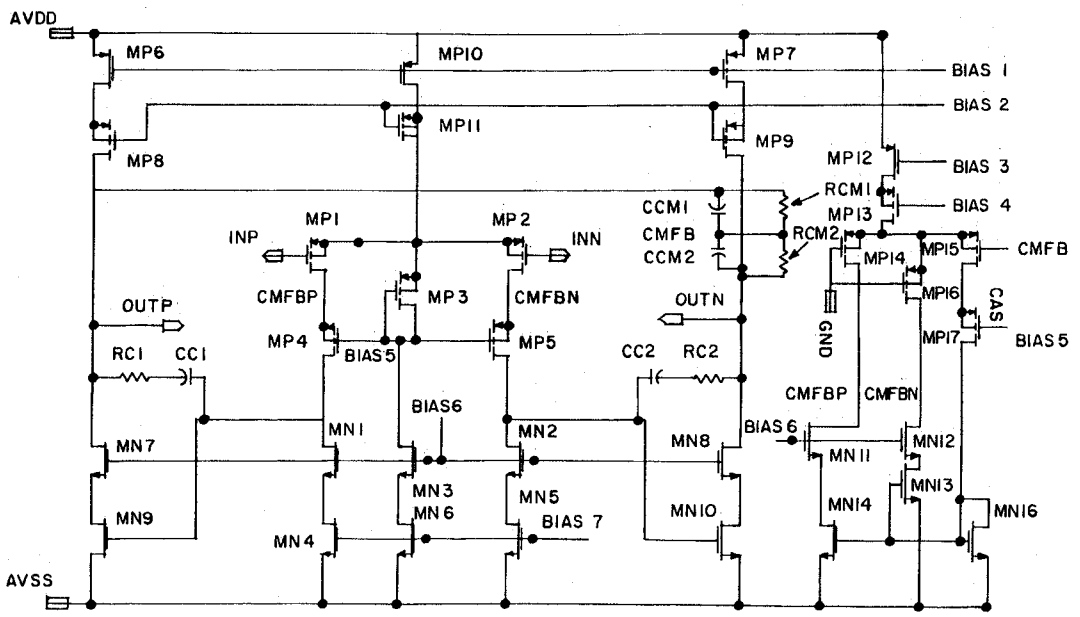


Fig. 6. Schematic diagram of 2-stage op amp.

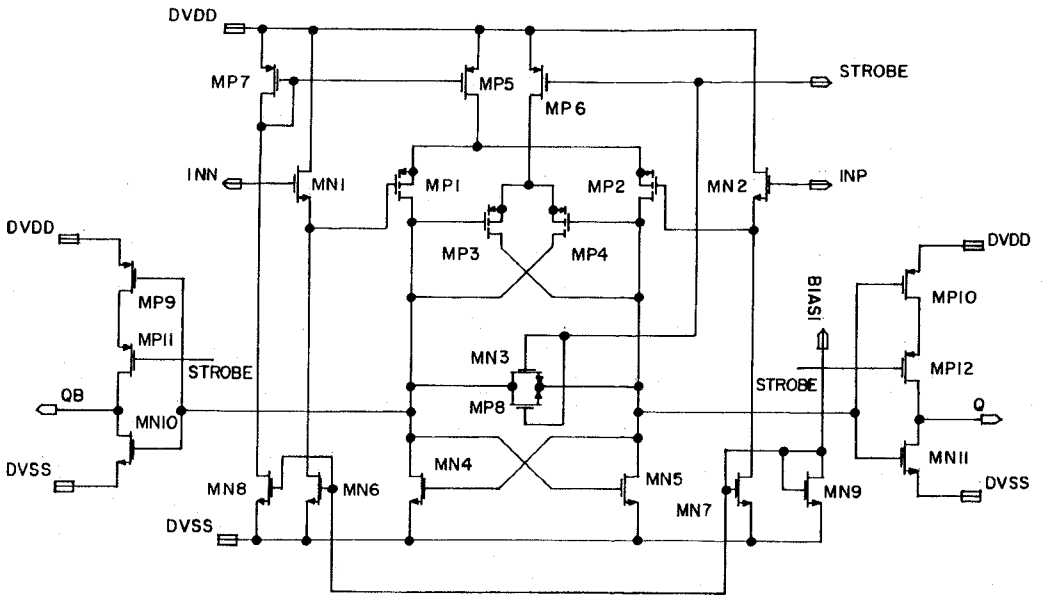


Fig. 7. Schematic diagram of comparator.

gives the offset due to charge injection referred to the input of the ith stage, $V_{\mathrm{OS}}(i)$. Next, V_{REF} is sampled on C_1, and 0 V is sampled on $C2$ as shown in Fig. 5(c). By forcing the bit to 1, $C2$ is connected to V_{REF}, and $C1$ is connected to the output giving the output voltage $V_{\mathrm{error}} = \alpha_i V_{\mathrm{REF}} + V_{\mathrm{OS}}(i)$ as shown in Fig. 5(d). This voltage is digitized by the following stages. By subtracting the offset measured previously, the value of α_i is obtained. It should be emphasized that the measurement of V_{OS} and V_{error} does not depend on prior calibration of other stages. This is because both V_{OS} and V_{error} are small quantities, and the following stage decisions will be 0, so the result will get multiplied by 2 without the addition or subtraction of V_{REF}, until the result reaches the last few stages where the bit decisions are 1's or -1's. The gain errors in other stages therefore contribute only negligible gain error in the measurement of α_i. The offset errors of other stages are indistinguishable from the offset $V_{\mathrm{OS}}(i)$ of the current stage, the effect of which is removed as described earlier. For this reason, the calibration of one stage can be performed without calibrating other stages. This also avoids accumulation of errors in the correction terms. The 1.5 b/stage algorithm not only make the digital calibration possible, but also makes

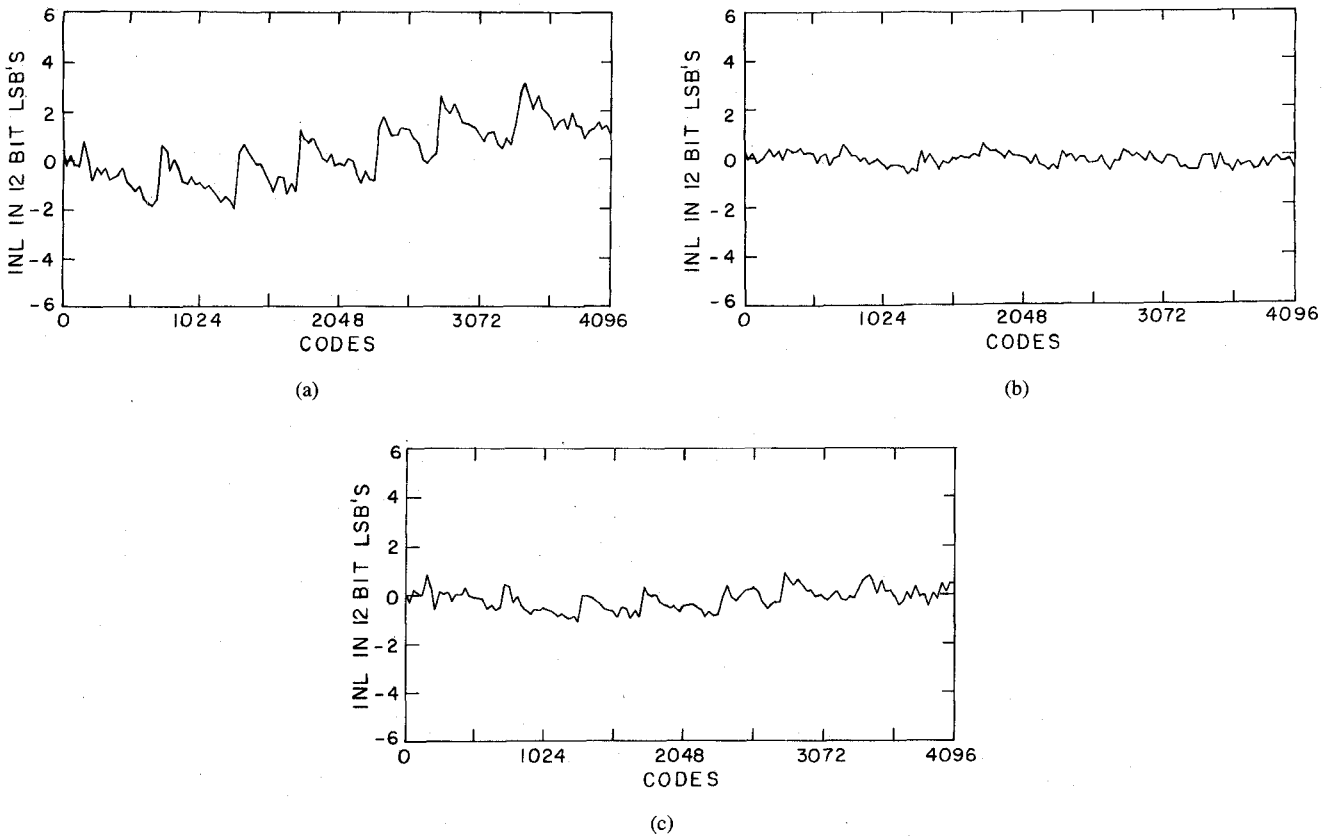


Fig. 8. Integral nonlinearity (a) before calibration, 600 ks/s, (b) after calibration, 140 ks/s, (c) after calibration, 600 ks/s.

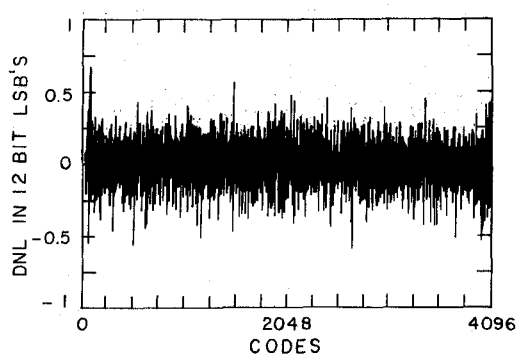


Fig. 9. Differential nonlinearity.

each stage calibration independent of other stages. This is particularly important for the calibration of cyclic converters where the measurement of error in a stage requires the use of the same stage (uncalibrated) in a cyclic manner.

The overall input referred offset can be easily measured and calibrated by applying 0 V at the input of the converter and digitizing it. The digitized offset is stored in RAM and subtracted from each conversion result during the normal conversion cycles.

V. Prototype Converter Circuits

To demonstrate the concept of calibration, a prototype 2-stage A/D converter has been implemented in a standard 1.6-μm CMOS process. In the prototype converter, the output of the second stage is fed back to the first stage for a pipelined cyclic operation. Seven clock cycles are needed for a 14-b raw result which is subsequently calibrated and truncated to 12 b. As shown in Fig. 3, each stage consists of 2 capacitors of 1 pF each, an operational amplifier and two comparators. Fig. 6 shows the schematic diagram of the operational amplifier used in the converter. A 2-stage design is chosen to obtain open loop gain greater than 80 dB to reduce the linearity error due to the finite gain effect. Both the first and the second stage are cascoded for high gain. A continuous-time common-mode feedback circuit is employed. Polysilicon resistors R_{C_1} and R_{C_2}, 30 kΩ each, senses the output common mode. Although the effectiveness of the cascode in the second stage is reduced by the common-mode sensing resistors, gain is still higher with the cascode due to the low output resistance of short channel MOSFET's. The capacitors C_{CM1} and C_{CM2}, 1 pF each, introduce a zero in the common-mode transfer function to help stabilize the common-mode signal path. The common-mode amplifier consisting of MP12–17 and MN11–16 forces the output common mode to zero. The common-mode difference current generated by MP14 and MP16 is fed back to the input stage (via nodes labeled CMFBP and CMFBN) to regulate the output common-mode voltage. The pole-splitting compensation network (C_{c1}, C_{c2}, R_{c1}, and R_{c2}) stabilizes both the differential and the common-mode signal paths. The operational amplifier, using a 1.6-μm minimum gate

TABLE I
SUMMARY OF EXPERIMENTAL RESULTS

Resolution	12 b
Sampling rate	600 kS/s
Power supply	±2.5 V
Input range	±0.8 V differential
Power dissipation	45 mW
DNL	±0.6 LSB
INL	±1 LSB
Input referred noise	0.6 LSB rms

length, achieves 90-dB open-loop gain and 100-MHz unity-gain bandwidth.

Fig. 7 shows the schematic diagram of the comparator. When STROBE is high, the differential input is applied through MP1 and MP2, MP3 and MP4 are turned off, and the positive feedback in MN4 and MN5 is overcome by a CMOS switch MN3 and MP8. When STROBE is low, MP3 and MP4 are turned on, and MN3 and MP8 are turned off, and the latch regenerates rapidly. The input source followers (MN1, MN2, MN6, and MN7) serve two purposes. First, they reduce the kickback effect of the latch to the operational amplifier output. This is particularly important because the latch is activated before the operational amplifier has fully settled. A significant kickback would increase the settling time of the operational amplifier. Second, an offset of approximately 1/4 V_{REF} is introduced by using different W/L ratios for MN1 and MN2. This obviates the separate resistor string to set the comparator reference voltages (V_+ and V_-) in a conventional multistage converter, saving power and area. However, with this approach the comparator threshold will not be exactly 1/4 V_{REF}. The deviation of the comparator threshold from 1/4 V_{REF} reduces the margin of comparator error by the same amount from ± 1/4 V_{REF}.

VI. EXPERIMENTAL RESULTS

The output of the second stage is fed back to the first stage 7 times cyclically to obtain 14-b uncalibrated digital outputs which are calibrated and truncated to yield 12-b results. The logic circuit for the digital calibration was emulated by a computer program. The converter runs at a maximum of 4.2 MHz clock (600 kS/s sampling rate) in the cyclic mode, at 45-mW power.

Fig. 8 shows the integral nonlinearity (INL) before and after calibration. In Fig. 8(a), the converter shows ±2.5 LSB's of INL before calibration. After calibration, it is improved to ±0.5 LSB at 140 kS/s, and to ±1 LSB at 600 kS/s, respectively, as indicated in Figs. 8(b) and (c). The increase of INL at full speed is believed to be due to insufficient settling of the operational amplifier. Fig. 9 shows the differential nonlinearity (DNL) plot after calibration obtained by code-density measurements with the converter operating at full speed. The maximum DNL is shown to be 0.6 LSB's. The DNL peaks near the negative and the positive full scales are due to the amplitude of the ramp which is slightly less than the full scale. The total input referred offset before calibration is 12 LSB's and is reduced to less than 1/2 LSB after calibration. The rms input referred noise was measured to be 0.6 LSB which was considerably larger than the simulated value. The source of extra noise is not clearly understood yet. The die photograph is shown in Fig. 10. The active die area is 1 mm^2 (1600 mil^2). Table I summarizes the experimental results.

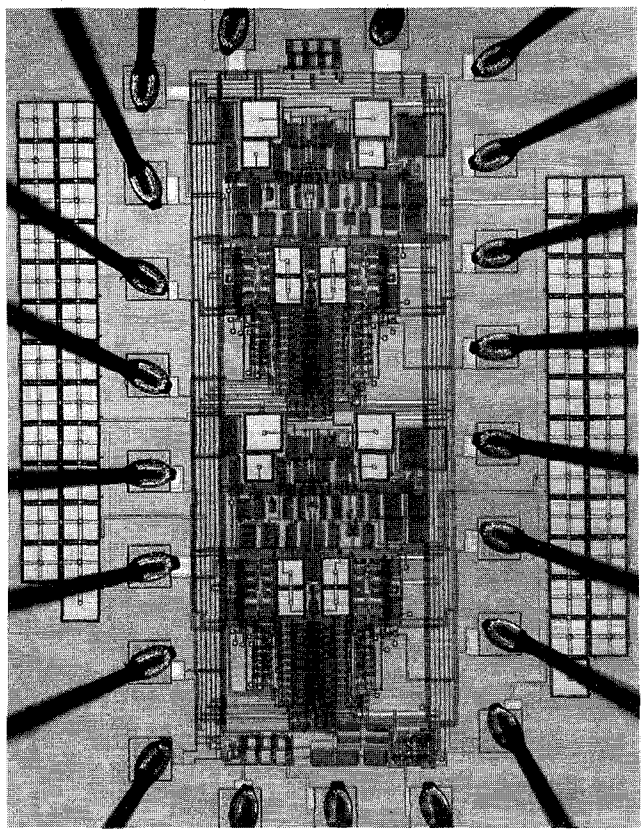


Fig. 10. Die photograph.

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