CMOS Resistive Fuses for Image Smoothing and Segmentation

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***Abstract*—A two-terminal nonlinear element called a resistive fuse is described. Its application in image smoothing and segmentation is explained. Two types of CMOS resistive fuses were designed, fabricated, and tested. The first implementation employs four depletion-mode NMOS and PMOS transistors, occupying a minimum area of 30 μm × 38 μm. The second implementation uses 7 or 11 standard enhancement-mode transistors on an area of 75 μm × 100 μm or less. Individual resistive-fuse circuits have been fabricated and tested and their functionality has been demonstrated. A one-dimensional network of 35 resistive fuses using the 11-transistor implementation was also fabricated in a standard CMOS process. Experimental results indicate that the network is capable of smoothing out small variations in image intensity while preserving the edges of objects.**

I. Introduction

In machine-vision applications, a large amount of data must be processed rapidly, posing a significant challenge in hardware implementation. Although digital processing is powerful and flexible, analog signal processing can operate at a higher speed for a given area and power [1], [2]. For early-vision[1] applications, analog processing is particularly useful since the vast amount of data is processed with a relatively low-precision requirement (typically 6–8 b) [3], [4]. After the amount of data is reduced by the early-vision stages, the subsequent middle- and late-vision tasks can be handled more easily by digital signal processing.

In this paper, we describe a nonlinear analog circuit called a resistive fuse for a particular early-vision task: image smoothing and segmentation.

Consider a typical one-dimensional continuous-space image signal such as the one labeled V_{in} shown in Fig. 1. The horizontal dimension represents distance and the voltage on the vertical dimension represents the image intensity. The abrupt step in the center of the signal corresponds to the edge of an object where there is a sharp intensity change. The small ripples in the two flat regions to the right and to the left of the step represent typical noise associated with a given image.

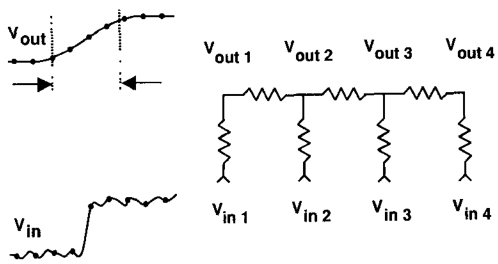

Fig. 1. A one-dimensional linear resistive network.

A. Smoothing

In many image processing applications, it is desirable to smooth out small variations of the intensity in the image. A spatial low-pass filter that performs a Gaussian or a binomial convolution of the image can be used for image smoothing [5], [6]. An interesting implementation of such a low-pass filter in one dimension is a linear resistive network, shown in Fig. 1, where V_{in} represents the image intensity from the original image and V_{out} represents the image intensity of the filtered image. Although V_{in} and V_{out} are drawn as continuous signals, they are actually discrete in space. It can be shown that in the continuous limit V_{out} is the spatial convolution of V_{in} with an exponential function given below [7]:

$$f(x) = \frac{1}{2L} e^{(-|x|/L)} \tag{1}$$

where

$$L = \frac{1}{\sqrt{\rho_h \sigma_v}}. \tag{2}$$

The quantities ρ_h and σ_v are the resistance and conductance per unit length in the horizontal and vertical dimensions, respectively. The quantity L is defined as the space constant. In the discrete case, the behavior is similar.

B. Segmentation

Unfortunately, such smoothing blurs the edges of objects in a given image, as evidenced by the broadening of the step in V_{out} shown in Fig. 1. Resistive-fuse networks have been proposed where the horizontal resistors in a

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[1]Here "early" refers to the stages of the processing that closely follow the stage of image acquisition using photodiodes, for example.

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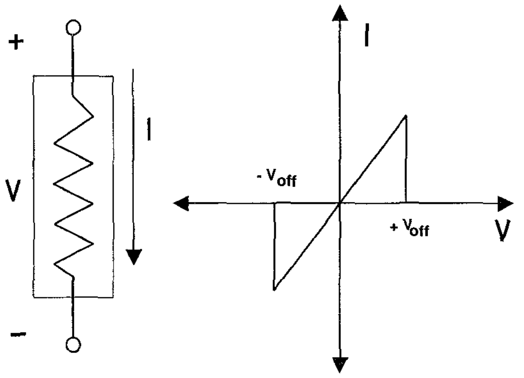

Fig. 2. The I–V characteristic of an ideal resistive fuse.

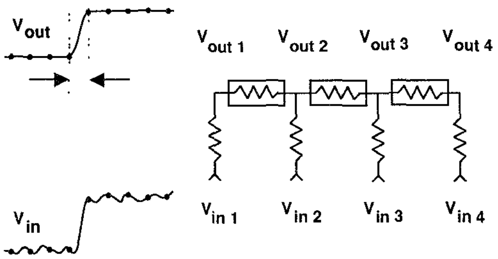

Fig. 3. A one-dimensional resistive-fuse network.

resistive grid are replaced by resistive fuses to perform image smoothing and segmentation [8], [9]. Fig. 2 depicts the I–V characteristic of an ideal resistive fuse. The breaking of a resistive fuse is nondestructive in that if the voltage across the fuse is reduced below V_{off}, the I–V characteristic returns to the linear characteristic.

Fig. 3 shows the one-dimensional implementation of the smoothing and segmentation network where the horizontal elements are resistive fuses and the vertical elements are linear resistors. For small intensity variations, the resistive fuses function as linear resistors, thus smoothing the image as in the conventional resistive network. However, when there is a large intensity difference between adjacent pixels, the resistive fuse *breaks*, becoming essentially an open circuit. There is no smoothing across the edge, as evidenced by the abrupt step in V_{out} shown in Fig. 3.

A two-dimensional grid that performs image smoothing when the horizontal elements are linear resistors or both image smoothing and segmentation when the horizontal elements are resistive fuses is shown in Fig. 4.

C. Examples of Smoothing and Segmentation Processing

To further motivate the design of resistive fuses, we present some images that are obtained using simulation software [10], [11]. The simulation was executed on a Connection Machine,[2] using a macromodel of the resistive fuse and the rectangular-grid structure shown in Fig. 4.

[2]Trademark of Thinking Machine Corporation, Cambridge, MA.

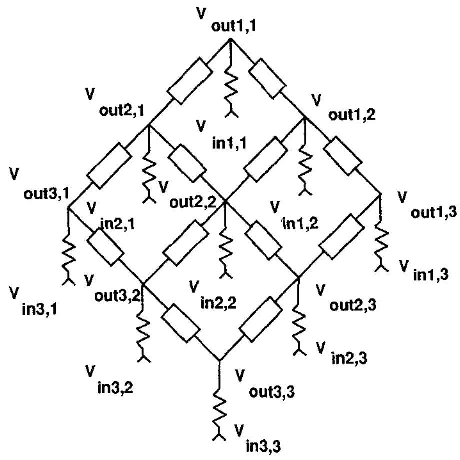

Fig. 4. A two-dimensional grid. The horizontal elements can be either linear resistors or nonlinear resistive fuses.

Fig. 5(a) shows the original 256 × 256 image of the San Francisco skyline taken from the digitized output of a CCD camera with 5 V being the full scale. Fig. 5(b) shows the *linear-resistive-grid* processed image. As one can see, small intensity variations such as windows on the buildings are smoothed out. However, as one may also expect, the edges of objects such as the buildings are also blurred.

Fig. 5(d) shows the *resistive-fuse-grid* processed image, when V_{off} is 50 mV. Small intensity variations such as windows on the dark sides of the buildings are smoothed out. At the same time, the outlines of objects such as the buildings remain sharp.

Fig. 5(d) shows the resistive-fuse-grid processed image, when V_{off} is 125 mV. Small intensity variations such as the windows on both sides of the buildings are almost completely smoothed out. As in the case of 50-mV V_{off}, the outlines of objects such as the buildings remain sharp.

From the images presented in Fig. 5 we see that resistive fuses can be used in the areas of image enhancement and image coding. In image-enhancement applications, if small intensity variations such as windows are considered noise, resistive-fuse processing can be used to smooth out the noise and can thereby increase the signal-to-noise ratio. In image-coding applications, resistive-fuse processing can be used to preserve only the essential features of an image such as the outlines of the buildings and can thereby reduce the number of pixels that have to be coded and transmitted.

We now consider the circuit implementations of resistive fuses. Previous implementations require a large number of MOS transistors per fuse (e.g., 33 transistors in [8]). In the following sections, we present a 4-, a 7-, and an 11-transistor fuse.

II. The Four-Transistor Fuse

A. Circuit Operation

The operation of the four-transistor resistive fuse can be understood from the behavior of the Chua resistor [12],

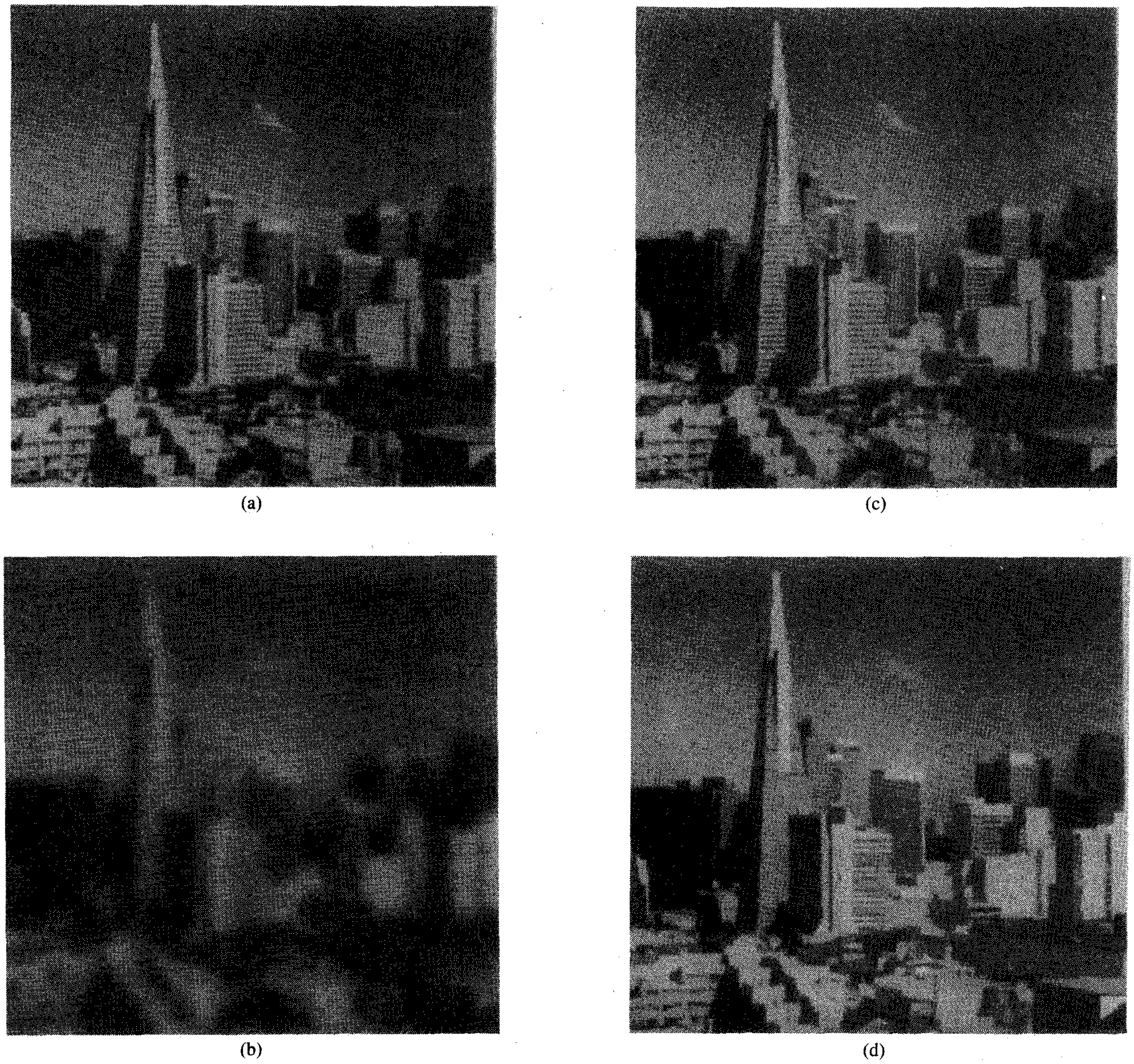

Fig. 5. Examples of linear resistive and resistive-fuse grid processing. (a) Original image of the San Francisco skyline. (b) Simulated result of a linear resistive grid. (c) Simulated result of a resistive-fuse grid with $V_{\text{off}} = 50$ mV. (d) Simulated result of a resistive-fuse grid with $V_{\text{off}} = 125$ mV.

shown in Fig. 6. The NMOS and PMOS transistors are depletion-mode devices, so the threshold voltage of the NMOS device is negative and the threshold voltage of the PMOS device is positive. The transistors are modeled using the usual square-law equations.

For simplicity, assume that $MN1$ and $MP1$ are complementary devices, so that

$$V_{T_p} = -V_{T_n} = V_T > 0 \tag{3}$$

and

$$k_p = k_n = k = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right). \tag{4}$$

The terminal voltages of the Chua resistor can be expressed as the sum of a common-mode signal and a difference-mode signal. To simplify the analysis, the common-mode signal is assumed to be zero. Common-mode variation of the actual I–V characteristic will be shown as part of the experimental results. The applied voltages are therefore taken to be purely differential as shown in Fig.

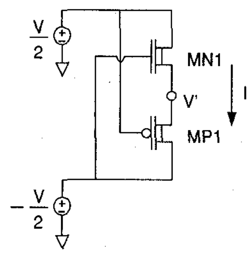

Fig. 6. The Chua resistor.

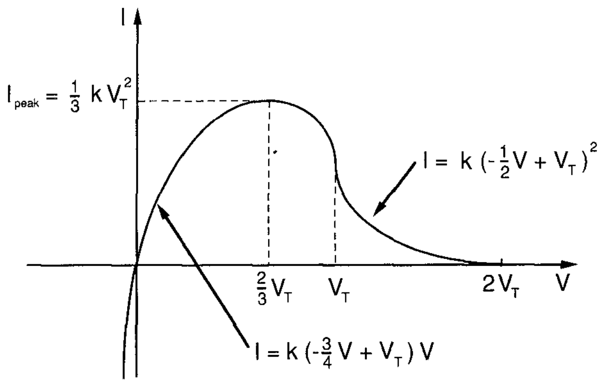

Fig. 7. The theoretical Chua resistor I–V characteristic.

6. Since $MN1$ and $MP1$ are complementary, $V' = 0$ by symmetry. This considerably simplifies the analysis of the Chua resistor since all terminals of $MN1$ and $MP1$ have known voltages. Examining $MN1$ in particular, we see that when $V = 0$, the drain current of $MN1$ is zero. For small applied voltages, $MN1$ is in the triode region and I is approximately proportional to V. As V increases in the positive direction, $MN1$ first saturates, then shuts off completely since its gate–source voltage V_{GS} constantly decreases. As V increases in the negative direction, $MN1$ remains in the triode region and becomes more conductive because its V_{GS} constantly increases. Analysis shows that $MN1$ is in the triode region when $V < V_T$, saturated when $V_T < V < 2V_T$, and cut off when $V > 2V_T$. The current I through the Chua resistor is given by

$$I = k(-\tfrac{3}{4}V + V_T)V, \qquad \text{for } V < V_T \tag{5}$$

and

$$I = k(-\tfrac{1}{2}V + V_T)^2, \qquad \text{for } V_T < V < 2V_T. \tag{6}$$

A peak current of $I_{\text{peak}} = (1/3)kV_T^2$ occurs when $V = (2/3)V_T$ and the conductance at the origin is kV_T. The complete I–V characteristic is shown in Fig. 7.

The resistive fuse is obtained by placing two Chua resistors back-to-back as shown in Fig. 8. Again, we assume that the PMOS and NMOS devices are complementary. For $V > 0$, the Chua resistor formed by $MN2$ and $MP2$ is operating in its high conductance region so that the overall characteristic of the resistive fuse closely follows the Chua resistor characteristic of $MN1$ and $MP1$. The resistive fuse is symmetrical, so its I–V characteristic must also be symmetrical. SPICE simulation of a sample I–V characteristic, assuming a V_T of 2 V, is shown in Fig. 9.

B. Experimental Results

The resistive fuse described above has been fabricated at the M.I.T. Microsystems Technology Laboratories in a variant of the M.I.T. 1.75-μm twin-well CMOS process. The depletion-mode devices were produced by ion implantation of appropriate dopants. The implant doses used resulted in substantial mismatches in the thresholds

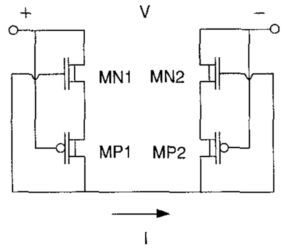

Fig. 8. A four-transistor resistive fuse.

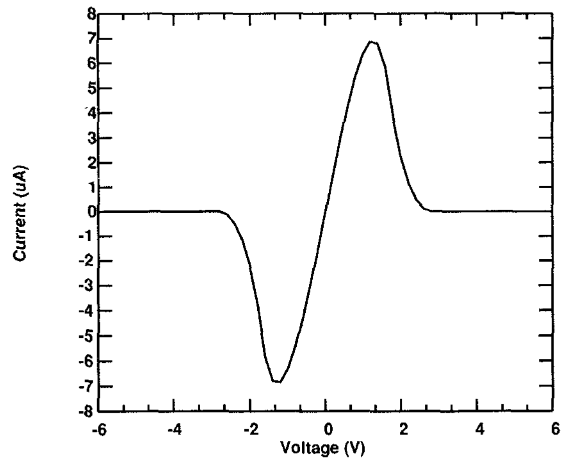

Fig. 9. Simulated I–V characteristic of the four-transistor fuse with complementary NMOS and PMOS transistors.

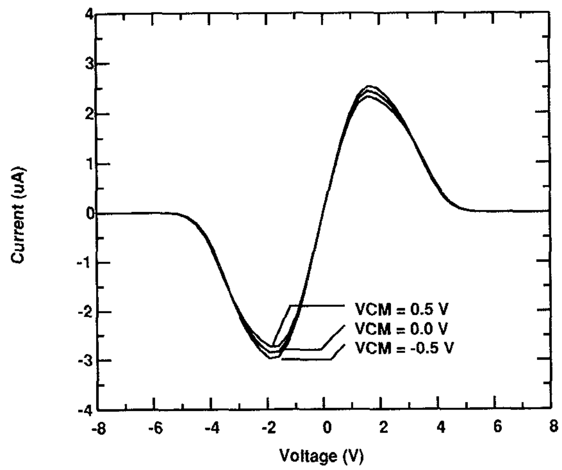

Fig. 10. Experimental I–V characteristics of the four-transistor fuse.

of the NMOS and PMOS devices. The zero-bias (i.e., zero source-bulk voltage) threshold of the NMOS devices was found to be about −2.3 V and the zero-bias threshold of the PMOS devices was found to be about 4.7 V.

Despite the threshold mismatch, the circuit still behaves qualitatively as predicted. A family of experimental I–V characteristics for common-mode voltage (V_{CM}) levels of −0.5, 0, and 0.5 V is shown in Fig. 10. Common-mode variation can be further reduced when the thresholds of the NMOS and PMOS devices are better matched.

Fig. 11 shows a photograph of the four-transistor fuse.

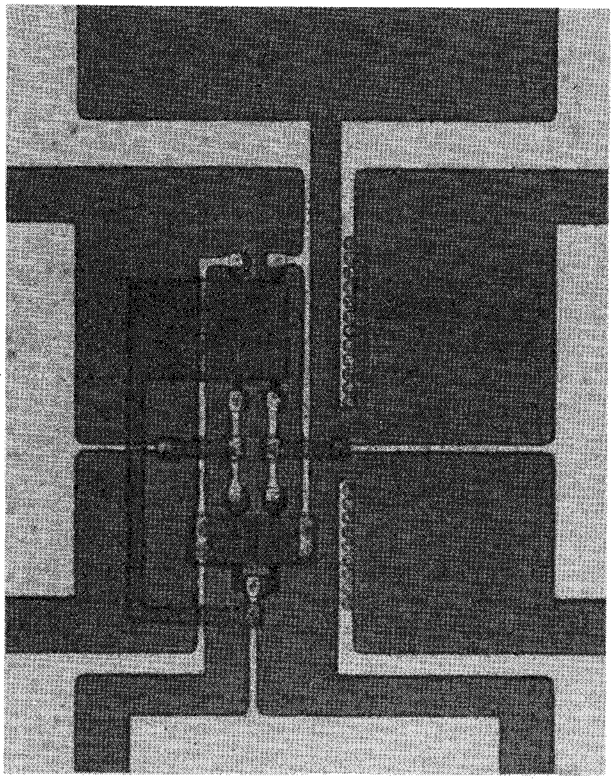

Fig. 11. Photograph of the four-transistor fuse.

III. The 7- and 11-Transistor Fuses

Although the resistive fuse described above uses only four transistors, it requires process modification to accommodate depletion-mode transistors and its behavior is not adjustable. In this section, an alternate approach is described that uses a standard CMOS process and allows electronic control of the linear-region resistance R_{EQ} and V_{off}. By varying R_{EQ}, one controls the space constant L and thus the degree of smoothing. By varying V_{off} between a large and a small value, one controls what edge heights (i.e., intensity jumps) are preserved. For large V_{off}, only steep edges are preserved, while for small V_{off}, shallow edges are preserved as well. Furthermore, because fuse networks often have multiple solutions, it is useful to vary V_{off} in time while processing a single image. The time interval over which V_{off} is varied should be several times longer than the settling time (10 μs, see Section IV), but much shorter than the time over which a typical input image varies significantly. Simulations have shown that initially setting V_{off} high and then reducing it to the final value typically causes the network to settle into the desired final state [13].

A. Circuit Operation

The basic circuit diagram of the seven-transistor fuse is shown in Fig. 12, where the transistors are all enhancement mode. The transistors outside of the dashed box are global biasing transistors that are typically shared by many fuses and are thus not included as part of the transistor count. The two terminals of the fuse are at $V1$ and $V2$.

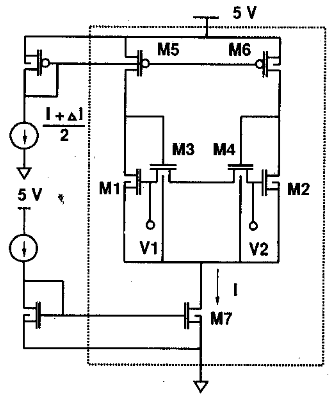

Fig. 12. A seven-transistor fuse.

Transistors $M1$ and $M2$ form a differential pair biased by transistor $M7$. Transistors $M5$ and $M6$ are biased such that their saturation currents I_{DS5} and I_{DS6} are larger than the quiescent bias currents of transistors $M1$ and $M2$:

$$I_{DS5} = I_{DS6} = \tfrac{1}{2}(I + \Delta I). \tag{7}$$

When no differential voltage is applied, the current I is divided equally between $M1$ and $M2$. Since the saturation currents I_{DS5} and I_{DS6} are larger than $(1/2)\,I$, $M5$ and $M6$ are in the triode region. The gates of $M3$ and $M4$ are pulled up close to V_{DD}, causing $M3$ and $M4$ to be in the triode region. The resistance of the fuse in the linear region is then given by the linear-region resistances of $M3$ and $M4$ in series:

$$R_{EQ} = \frac{1}{2k_3(V_{GS3} - V_T)} + \frac{1}{2k_4(V_{GS4} - V_T)} \tag{8}$$

where k_i is the same as k in (4).

We now consider the case when $V1$ is increased relative to $V2$. Increasingly more of the tail current I will be steered through $M1$. When the current through $M1$ exceeds I_{DS5}, the drain of $M5$ is pulled down from close to V_{DD} to close to the source potential of $M1$, turning $M3$ off, while $M6$ is still in the triode region. The off voltage V_{off}, which is the voltage across the fuse when either $M3$ or $M4$ turns off, can be found by equating the drain current of $M1$ or $M2$ to $(1/2)(I + \Delta I)$:

$$V_{\text{off}} = \pm \frac{\sqrt{I + \Delta I} - \sqrt{I - \Delta I}}{\sqrt{2k_{1,2}}}. \tag{9}$$

From (9), one can see that V_{off} can be controlled by varying I or ΔI. In addition, since the circuit is symmetrical, the I–V characteristic is symmetrical as desired.

Although the basic circuit in Fig. 12 functions as a resistive fuse and may be used in some applications, there are a few drawbacks. From (8), it can be seen that R_{EQ} depends on V_{GS3} and V_{GS4}, indicating a high common-mode sensitivity. Since R_{EQ} is otherwise fixed once the circuit is fabricated, the circuit offers no electronic control of R_{EQ}, except for the undesired variation due to the common-mode voltage.

The 11-transistor fuse shown in Fig. 13 improves on

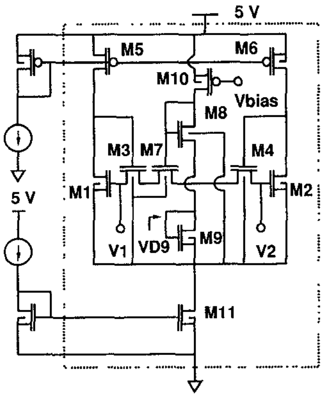

Fig. 13. An 11-transistor fuse.

the 7-transistor fuse. As in the case of the 7-transistor fuse, the transistors outside of the dashed box are global biasing transistors and thus not included as part of the transistor count.

The resistances of $M3$ and $M4$ are made small compared to the resistance of $M7$ by using the appropriate aspect ratios. Since the resistance of the fuse is dominated by the resistance of $M7$ in the triode region, the fuse resistance is set by the ON-resistance of $M7$. $M8$ through $M10$ bias the gate of $M7$ so that $V_{GS7} - V_T$ is kept constant over the common-mode range, making the ON-resistance insensitive to the common-mode voltage. R_{EQ} can be electronically controlled by varying the current flowing through $M10$ and thus changing the gate voltage of $M7$.

Biasing transistor $M10$ such that its drain current equals the saturation currents I_{DS1} and I_{DS2}, one can show that, neglecting second-order effects such as channel length modulation, $V1 = V2 = VD9$ when there is no differential voltage applied to the fuse. It follows that

$$V_{GS7} - V_T = V_{GS8} - V_T = \sqrt{\frac{I_{DS10}}{k_8}}. \tag{10}$$

Thus the linear resistance R_{EQ} is

$$R_{EQ} \simeq R_{ON7} = \frac{1}{2k_7}\sqrt{\frac{k_8}{I_{DS10}}}. \tag{11}$$

Equation (11) shows that R_{EQ} is adjustable by varying I_{DS10} and is independent of the common-mode voltage.

B. Experimental Results

The 11-transistor fuse in Fig. 13 was fabricated in a standard 2-μm p-well CMOS process through MOSIS. Transistors $M1$ and $M2$ used in the differential pair have a W/L ratio of 15/6, while the PMOS transistors $M5$ and $M6$ have a W/L ratio of 10/6. All measurements were obtained using a single power supply of 5 V.

Fig. 14(a) shows the I–V characteristics of the 11-transistor fuse at two current levels differing by a factor of 10. Note that $I_{DS1,2}$, $I_{DS5,6}$, and I_{DS10} are changed proportionally. It can be seen that R_{EQ} can be varied from approximately 300 kΩ to 5 MΩ, a factor of 16. This factor is significantly more than the factor of 3.16 predicted by (11) because the transistors are operating in or near the subthreshold region rather than the square-law region assumed in deriving (11). In principle, R_{EQ} can be changed while keeping V_{off} constant by changing I_{DS10} while keeping $I_{DS1,2}$ and $I_{DS5,6}$ constant. Note also that the I–V characteristics are close to ideal.

Variability in V_{off} from 40 to 120 mV is shown in Fig. 14(b). Since the current through the fuse is small (on the order of 10 nA), the $V_{D,SAT}$ of $M7$ is small. As a result, when $V_{DS7} \simeq |V1 - V2|$ increases beyond about 50 mV, the resistance of $M7$ becomes nonlinear.

Fig. 14(c) shows the I–V characteristics over the common-mode range of 1.2 to 2.7 V. The slight raggedness of the I–V characteristic near the origin is due to the extremely small current levels (1 nA) approaching the resolution limit of the instrument used in the measurement.

The changes in V_{off} and R_{EQ} are due to the finite output resistances of transistors $M1$, $M2$, $M5$, and $M6$. Consider the case when the differential voltage applied to the fuse is small. Since the gate voltages of $M3$ and $M4$ are close to V_{DD}, as one increases both $V1$ and $V2$, it becomes increasingly easier to turn off either $M3$ or $M4$, depending on the polarity of the differential voltage. As a result, as one raises the common-mode voltage, V_{off} decreases. Similarly, the variation of R_{EQ} is caused by the variation of $V_{GS7} - V_T$, due to the finite output resistances of $M10$ and $M11$.

The common-mode sensitivity of V_{off} and R_{EQ} can be reduced by using longer channel transistors and/or cascoding at the cost of more area. This trade-off becomes a system-level issue as one tries to maximize the size of the rectangular grid by minimizing the area per fuse while keeping the I–V characteristics insensitive to the common-mode variation. As a related system-level issue, it should be noted that when building a large grid of fuses, the primary impact of transistor mismatch is on the off-voltage due to the offset voltage of the differential pair used in the fuse. However, we expect the effect to be small, especially when V_{off} is large. Table I summarizes the measured performance of the 11-transistor fuse.

To demonstrate the resistive-fuse network functionality, a one-dimensional 36-node resistive-fuse network using the 11-transistor fuse has been built on the same chip. In Fig. 14(d) the input signal is shown as the noisy dashed line. By adjusting $I_{DS5,6}$ to be more than twice the values of $I_{DS1,2}$, we can prevent the fuses from turning off. Under this condition, the network emulates a linear resistive network whose processed output is shown as the solid line with the solid square symbol. Reducing $I_{DS5,6}$, we can again have a resistive-fuse network whose processed output is shown as the solid line with the triangular symbol. As one can see, while both linear resistive and resistive-fuse networks are capable of image smoothing, the latter network does a much better job in preserving the edge as

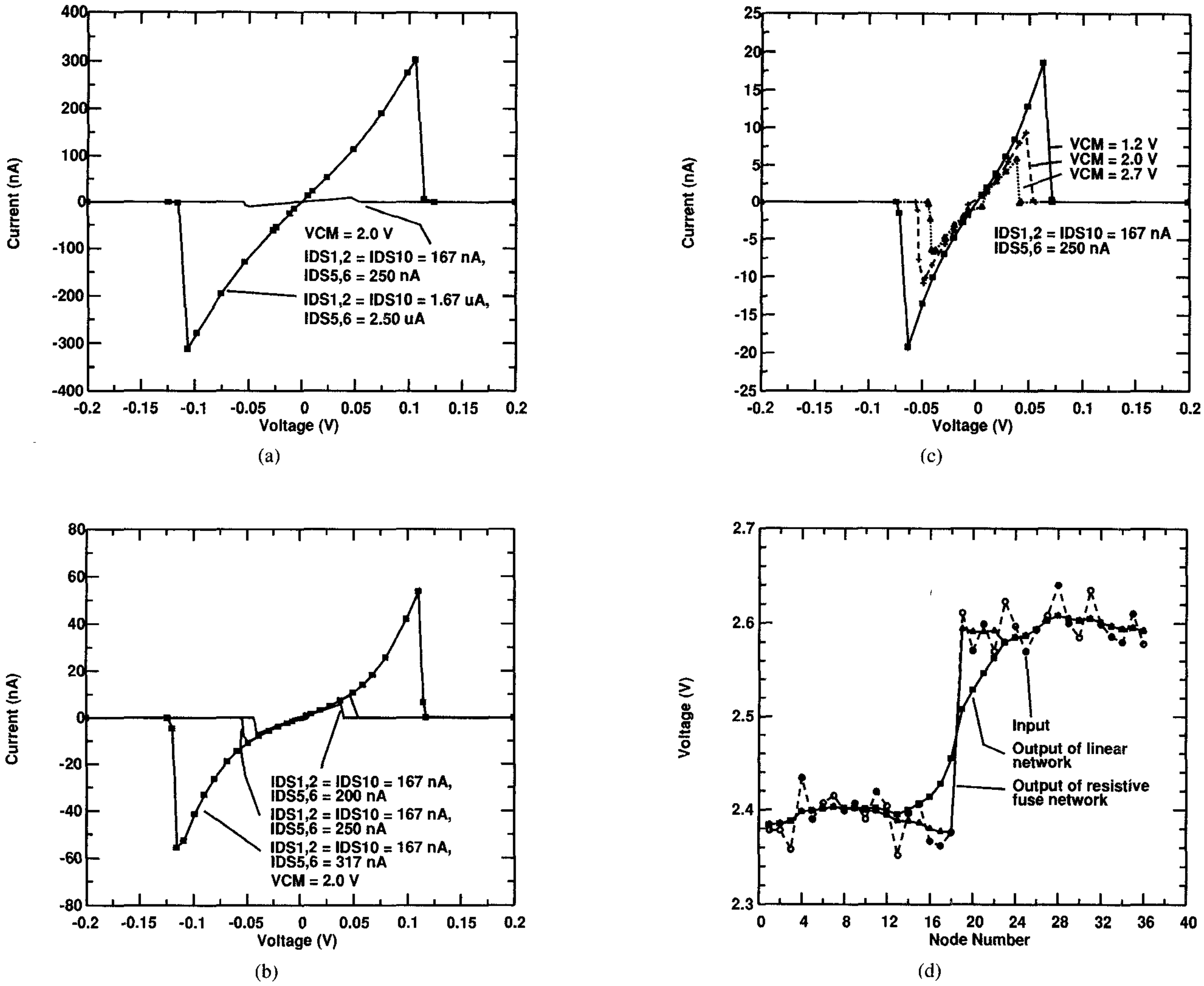

Fig. 14. Experimental results of the 11-transistor fuse and the 36-node one-dimensional network. (a) Variability of R_{EQ} (b) Variability of V_{off}. (c) Sensitivity of the I-V characteristics to common-mode voltage. (d) Input and output voltages of the one-dimensional network.

TABLE I
PERFORMANCE SUMMARY OF THE 11-TRANSISTOR FUSE

Resistance Variability	Factor of 16
Off-Voltage Variability	40–120 mV
Common-Mode Range	1.5 V
Area per Fuse	75 μm × 100 μm
Number of Transistors per Fuse	11
Power Dissipation per Fuse	2.5 μW (typical)

evidenced by the sharp transition. This experimental result agrees with the theoretical result shown in Figs. 1 and 3.

Fig. 15 shows a photograph of the 36-node one-dimensional resistive-fuse network.

IV. Some General Comments on the Resistive-Fuse Processing System

We will make some general system-level observation on the analog approach of resistive-fuse processing versus the digital approach. One should note, however, that such a comparison is very indirect and approximate because the direct implementation of the resistive-fuse function in a digital form would require iteratively solving a large coupled nonlinear set of equations, resulting in an impractical number of operations.

We first examine the expected performance of a fuse chip. A conservative bound on the settling time of a fuse grid is the time required for the parasitic capacitance at a single node to charge or discharge through the vertical resistor, neglecting the coupling through the fuses to the neighboring nodes. With a 1-MΩ equivalent resistance and a 1-pF parasitic capacitance looking into a node, we get a characteristic time constant of 1 μs. Therefore, we expect the resistive-fuse system to have a processing time of less than 10 μs. Typically, it is advisable to use some continuation method to prevent the resistive-fuse network from settling to a local minimum rather than to the desired global minimum [13]. It is estimated that the processing time will be increased by a small factor (e.g., 3 to 4) if the continuation method is employed. With some area optimization, it should be possible to build a 100 × 100 fuse-processing system on a 1-cm × 1-cm die with

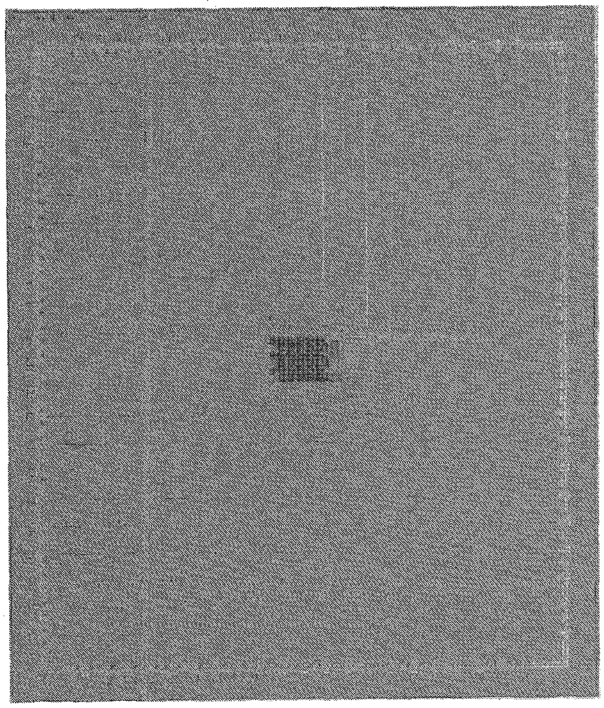

Fig. 15. Chip photograph of the one-dimensional network.

on-chip imager using a 0.7-μm CMOS technology. Since the typical power dissipation per fuse is 2.5 μW, the total power dissipation of such a chip would be less than 100 mW. Such an image size should be sufficient for most early vision tasks.

In order to make a reasonable comparison between a resistive-fuse system and a digital system, we have chosen two commercial digital chips [14] that we believe are the closest counterparts to the resistive-fuse chip. Both chips are fabricated with a 0.7- or a 0.9-μm CMOS technology. The first chip, L64240 from LSI Logic Corporation, can be configured as a two-dimensional transversal filter that can be used for edge detection. The transversal filter can segment a 100×100 image with 8 b/pixel in about 1 ms. The typical operating power is 2.5 W with a 20-MHz clock. The second digital chip, L64220, is a rank-value filter configured as a median filter. Using a moving 5×5 pixel window, it is also capable of processing a 100×100 image in about 1 ms. The typical operating power is 1.5 W with a 20-MHz clock. It should be noted that the speed and power performance of these two chips does not include the time and power required to digitize the input analog image signals.

From these figures, we can conclude that the resistive-fuse network operates one to two orders of magnitude faster and consumes an order of magnitude less power. We emphasize that digital systems do offer many advantages that analog systems do not offer, such as arbitrary precision level, more flexibility, and capability of complex processing. However, in early-vision applications, where the processing required tends to be simple, and 6- to 8-b precision seems sufficient, analog systems can offer potential advantages such as speed and power. We believe that perhaps an ideal system is one with an analog system at the front end, reducing the image to a suitable form which can then be subjected to more complex and precise digital processing.

V. Conclusion

We have designed, fabricated, and tested two types of compact CMOS resistive-fuse circuits for simultaneous image smoothing and segmentation. The first implementation, which uses four depletion-mode NMOS and PMOS transistors, has been fabricated in a modified 1.75-μm CMOS process. The basic functionality has been demonstrated. The second implementation using 11 enhancement-mode transistors was fabricated in a standard 2-μm CMOS process through MOSIS. Although physically larger than the four-transistor circuit, it offers electronic control of the smoothing threshold V_{off} and the space constant L through R_{EQ}. In addition, the one-dimension resistive-fuse network was also tested and found to be capable of smoothing out noise without blurring the edge.

Acknowledgment

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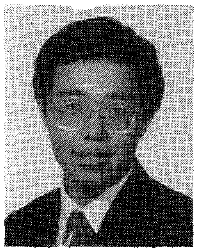

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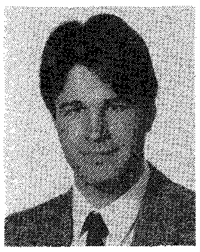

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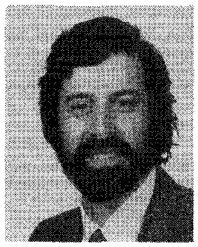

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about 1 ms. The typical operating power is 2.5 W with a 20-MHz clock. The second digital chip, L64220, is a rank-value filter configured as a median filter. Using a moving 5 × 5 pixel window, it is also capable of processing a 100 × 100 image in about 1 ms. The typical operating power is 1.5 W with a 20-MHz clock. It should be noted that the speed and power performance of these two chips does not include the time and power required to digitize the input analog image signals.

From these figures, we can conclude that the resistive-fuse network operates one to two orders of magnitude faster and consumes an order of magnitude less power. We emphasize that digital systems do offer many advantages that analog systems do not offer, such as arbitrary precision level, more flexibility, and capability of complex processing. However, in early-vision applications, where the processing required tends to be simple, and 6- to 8-b precision seems sufficient, analog systems can offer potential advantages such as speed and power. We believe

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