A 9-b Charge-to-Digital Converter for Integrated Image Sensors

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Abstract—**Charge-to-digital conversion offers advantages over conventional charge readout techniques because it performs digitization directly in the charge domain. The approach consolidates hardware, reduces power and weight, and eliminates many sources of noise and nonlinearity. This paper introduces an architecture for a charge-to-digital converter (CDC) that is tailored toward a charge-coupled device (CCD) implementation. New methods of generating charge, sensing charge, and comparing charge packets are described that improve conversion accuracy. Factors limiting device performance are discussed. Measured results are presented for two prototype CDC's. The first, using buried channel CCD's, is optimized for resolution. It achieves 56 dB spurious free dynamic range (SFDR) at a 2 MHz sampling rate and operates from 5 V. The second, using surface channel CCD's, is optimized for power and speed. It achieves 49 dB SFDR at a 15 MHz sampling rate and consumes 13 mW power at its maximum sampling rate of 22 MHz.**

I. Introduction

FULLY-INTEGRATED focal-planes are desirable to reduce the power, weight, and cost of imaging systems and to increase their flexibility and robustness. An integrated focal-plane includes all video signal readout and digitization circuits directly on-chip. A/D conversion occurs immediately after signal retrieval and all remaining communication is strictly digital. It is difficult to achieve such system integration with conventional video readout techniques.

This paper presents an alternative technique for digitizing charge packets, referred to as charge-to-digital conversion (CDC), that is free from many difficulties experienced by conventional techniques. The technique is applicable to either imagers with charge-coupled device (CCD) readouts or to other processing circuits utilizing CCD's. An important advantage of this technique is that, in contrast to alternative methods of charge digitization, A/D conversion is performed in the charge, rather than the voltage, domains.

Digitizing charge quanta is conventionally performed by a multistage procedure such as that shown in Fig. 1(a). A charge packet, originating from a CCD register, is first dumped onto a preset capacitor whose voltage falls in proportion to the packet size. The resulting pulse is buffered, driven off-chip, and amplified. The signal is then sampled by a sample-and-hold and processed by correlated-double-sampling circuitry to suppress reset noise. Finally, the resulting voltage is digitized by an A/D converter.

This process entails translating a charge packet to an intermediate voltage, which must then be digitized. The resulting clocked voltage waveforms must be low noise and have short settling times. The process also involves converting a discrete-time signal to a continuous-time signal, which must then be resampled. These operations constitute a majority of the hardware, power, and complexity required for readout and each processing stage introduces additional noise and nonlinearity.

The digitization process can be consolidated by utilizing the configuration shown in Fig. 1(b) and computing a digital representation of the charge signals on-chip, directly in the charge domain. In this method, charge packets are transferred directly from a CCD register into a CDC that is implemented using CCD elements. Signals continue as discrete-time charge quanta throughout the conversion process and no charge-to-voltage translation or resampling occurs. Consequently, circuits for voltage amplification, signal buffering, resampling, and correlated-double-sampling are unnecessary.

II. Converter Architecture

Only a limited set of operational building blocks are available for implementing an A/D converter in CCD technology [1]. Charge packets may be held, transferred between contiguous wells, and added with extreme precision. Accurate fixed-ratio charge division is also possible. The implementation of each of these operations is simple and requires only dynamic switching power. However, other operations such as subtraction, amplification, and nonadjacent transfers are less accurate and more difficult to implement.

Two CCD-based A/D converters have previously been reported with approximately 4-b performance [2], [3]. The limited accuracy of these devices is primarily due to two factors. Their architectures are oriented toward a CMOS implementation and require operations, such as subtraction, that are not accurately achieved using CCD's. Secondly, their circuit techniques for implementing charge sensing and comparison rely on accurate charge-to-voltage translations.

A fully-differential, bit-serial, successive approximation architecture, similar to that of the current CDC, was first described in [4]. However, the practical resolution of this device is limited by two factors. First, its comparators must be located asymmetrically, outside the CCD channels and this placement reduces the accuracy of its charge comparisons. Secondly, an accumulation of common-mode charge with

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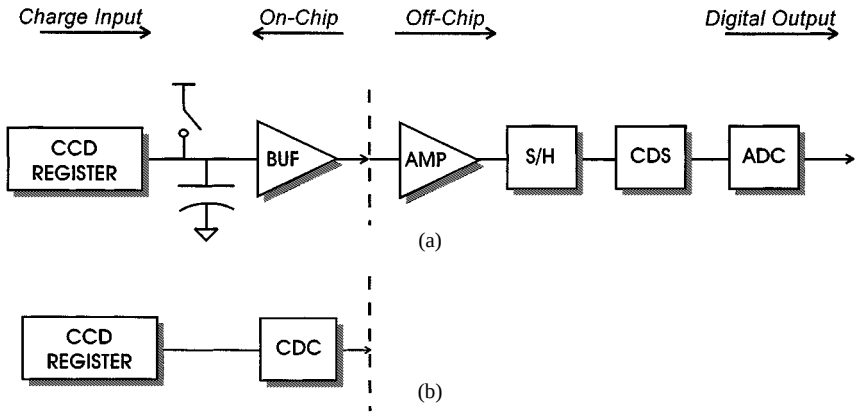


Fig. 1. Comparison of charge digitization procedures. (a) Conventional technique. (b) Direct charge-to-digital conversion.

each processing stage causes saturation in its charge sensing operations and amplifies channel mismatches.

The present CDC architecture is specifically tailored toward a CCD implementation and toward the pipelined nature of CCD operations. An N-bit converter, shown schematically in Fig. 2(a), contains a pipeline of N identical conversion blocks, through which a digital result is determined successively, from the MSB to the LSB, in a bit-serial manner. The pipeline is symmetrically divided into positive and negative halves. Each half consists of two charge flow channels, referred to as the accumulator and scaling channels. The channels begin at the converter inputs, pass through all conversion blocks in the pipeline, and terminate after the final block at charge drains. Each conversion block receives signals from its immediate predecessor, operates on these signals, and passes them on to the subsequent block. Multiple inputs are processed in parallel along the pipeline so that one digital word is completed each clock cycle.

The contents of a single conversion block are shown schematically in Fig. 2(b). The elements labeled D indicate delays and physically correspond to a set of CCD gates. The additive elements indicate charge summation and correspond to CCD wells that accept charge from two sources. The pairs of elements labeled 1/2 indicate fixed-ratio charge division and are implemented as CCD gates that transfer charge into two receiving wells in equal proportions. Switch elements represent conditional charge transfers and are accomplished by CCD gates that either pass or block charge flow.

The converter's first block accepts the differential signals to be digitized, s^+ and s^-, into the two accumulator channels and full-scale reference signals of equal size, g, into the two scaling channels. A comparison is performed on the accumulator charges, and the resulting output bit, representing the sign of their difference, is latched

$$\begin{aligned} d[m] &= 1, \quad \text{if } s^+[m] > s^-[m] \\ \overline{d[m]} &= 1, \quad \text{if } s^+[m] < s^-[m]. \end{aligned} \tag{1}$$

At the same time, the two scaling charges are each divided in half. The comparator's digital output is used to direct half of the scaling packet on either the positive or negative side, whichever contains less charge, to be added to its associated

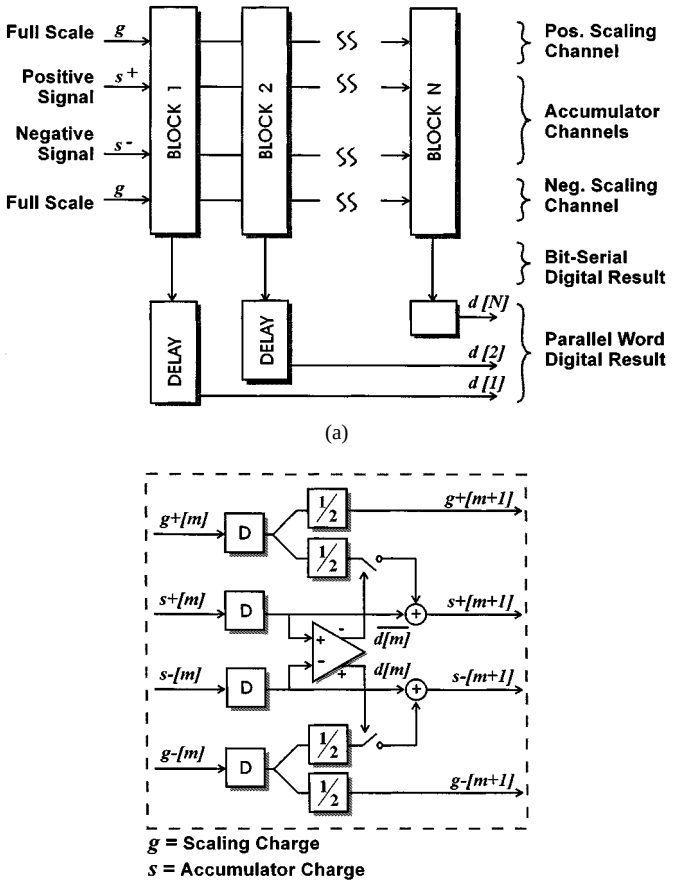


Fig. 2. Block diagram of CDC architecture. (a) N-bit pipeline. (b) Conversion block contents.

accumulator packet

$$\begin{aligned} s^+[m+1] &= s^+[m] + \overline{d[m]} \cdot 2^{-m} g \\ s^-[m+1] &= s^-[m] + d[m] \cdot 2^{-m} g. \end{aligned} \tag{2}$$

After these conditional summations, all resulting signals are passed forward and the same process is repeated at each conversion block along the pipeline.

The converter's digital result is constructed directly from a bit-shifted, weighted sum of the comparator outputs at each

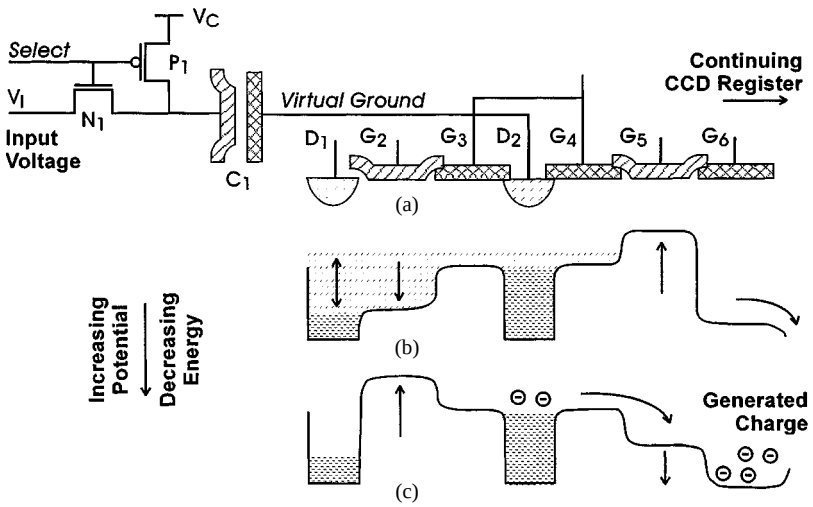


Fig. 3. Input charge generator. (a) Circuit configuration. (b) Precharge phase. (c) Sensing phase.

stage

$$s^+ - s^- = g \cdot \left(\sum_{m=1}^{N} 2^{-m+1} d[m] - 1 \right). \tag{3}$$

It represents, in an offset binary format, the number of LSB's spanned by the differential input signals. Although output bits are generated serially, additional digital reformatting latches may be included, as shown in the figure, to delay earlier bits and produce a parallel-word result.

The CDC may be operated with various input configurations in addition to that described above. One of the differential accumulator inputs may receive a constant signal for single-ended operation or to accomplish offset subtraction. This signal may also be varied each cycle to achieve adaptive offset adjustment. The scaling inputs, which determine the converter's gain, may also be varied to achieve adaptive dynamic range adjustment, calibration, or a piecewise linear or companding conversion characteristic.

The present architecture is well suited to a CCD implementation in the following ways. First, only operations of sampling, shifting, addition, and division by two are required, all of which are easily and accurately implemented using CCD's. The need for subtraction, present in a single-ended architecture, is eliminated by performing complementary addition. Second, an entirely charge-domain signal path is possible because connections only exist between neighboring CCD wells.

The third advantage occurs because duplicate scaling channels are located outside the two accumulators. This allows improved comparator performance for two reasons. Matching is enhanced because comparator preamplifiers are located symmetrically within the CCD channels, between the accumulators. Second, an entirely dynamic sensing, feedback, and comparison path, such as that described in the next section, is possible because preamplifiers neighbor charge sensing elements.

III. Charge-Domain Implementation

A. Charge Generation Circuits

Although a CDC is aimed at processing charge packets, it can accept voltage signals as well if an initial charge generation stage is included in series with each input. Common charge generation techniques are unacceptable because they provide less than 7-b linearity [5]. The present device utilizes an alternative technique, referred to as cascode charge generation, to achieve improved linearity. This circuit, shown in Fig. 3, consists of a polysilicon capacitor, C_1, connected to a clamp and sample circuit and to the input of a CCD register. Gates G_3 and G_4, surrounding the register input, are held at a constant bias.

Circuit operation is illustrated by means of energy level diagrams in Fig. 3. The precharge phase in (b) begins when the potential on G_5 falls, thereby closing the sensing path, and that on G_2 rises, opening the precharge path. Diffusion D_1 is initially pulsed low to replenish charges lost from D_2 during the previous cycle. D_1 is then returned high to remove excess charges and D_2's potential rises to the channel potential underneath barrier gate G_3. During this phase, P_1 holds C_1's input to positive clamp voltage, V_C.

The sensing phase in (c) begins when G_2 closes and G_5 opens. Transistor N_1 connects input V_I to C_1 and the change in voltage across this capacitor forces displacement current onto node D_2. As the potential on D_2 temporarily falls, G_4 can support current, charges are accumulated in the receiving well underneath gate G_6, and D_2 is gradually restored to its original precharge level.

During the following precharge phase, the generated packet

$$Q_0 = (V_C - V_I) \cdot C_1 \tag{4}$$

is transferred forward into the continuing CCD register.

This technique provides improved linearity for two reasons. First, its translation characteristic is based on highly linear polysilicon capacitance, C_1, rather than on CCD well capacitance. Second, static operation does not depend significantly on

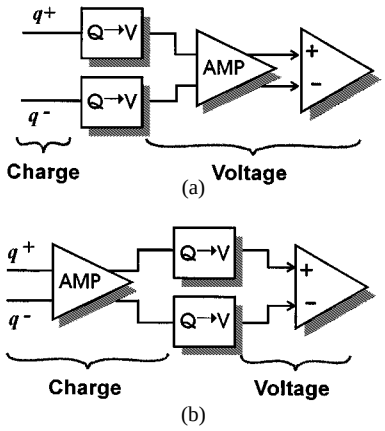


Fig. 4. Charge comparison techniques. (a) Voltage amplification. (b) Charge amplification.

any parasitic capacitances because D_2 has the same potential both before and after the sensing operation and functions as a virtual ground.

B. Charge Sensing and Comparison Circuits

As a result of the differential CDC architecture, common-mode charge accumulates with each pipeline stage. This accumulation is not a problem while signals remain in the charge domain, provided that CCD wells are sized to accommodate it. However, signals must eventually be translated to voltages for comparison. As a voltage, common-mode signal limits converter resolution.

Fig. 4(a) depicts typical charge comparison techniques. Two charges are independently translated to voltages and then provided to a preamplifier or comparator. High translation sensitivity is desirable for an LSB of differential to overcome inevitable comparator offsets. On the other hand, low translation sensitivity is required to assure that, as a voltage, the common-mode signal does not exceed power supply limits. Finally, accurate translation matching is necessary because mismatches are amplified by the common-mode signal. Together, these constraints dictate a maximum feasible converter resolution for this sensing technique of about 7 b [6].

The present device makes use of charge-mode amplification, depicted in Fig. 4(b), to achieve improved resolution. Two charges are jointly sensed by a charge-domain amplifier that amplifies desired differential and suppresses undesired common-mode before signals are translated to voltages at a comparator input. The advantages of this technique are the following. First, higher translation sensitivity is possible without the danger of saturation because common mode charge is reduced. Second, operation is less sensitive to translation mismatches. Finally, comparator resolution requirements are reduced by the additional charge-domain differential amplification.

Charge mode amplification is implemented by combining two differential charge replicators in a cross coupled fashion. The structure and associated energy diagrams for one such replicator are shown in Fig. 5. Although a replicator is largely similar to a cascode charge generator, described earlier, it differs in the following ways. First, its input signal is a charge packet that must be sensed multiple times and is needed by subsequent CCD elements. Floating gate G_1 is used to nondestructively sense this charge without altering it. Second, charge in the receiving well is sensed by floating gate G_7 and is fed back to gate G_5 in the opposite channel's replicator.

Differential charge replication is illustrated by means of energy diagrams in Fig. 5. The precharge phase in Fig. 5(b) presets floating gate, G_1, to the channel potential underneath gate G_3 in a manner identical to that described with reference to Fig. 3. Transistor N_1 is enabled during this time and receiving well gate G_7 is clamped to the bias on D_4 while the previous cycle's charge is removed from underneath it.

The sensing phase in Fig. 5(c) begins when G_2 closes the precharge path and G_6 opens the sensing path. Charge introduced underneath floating gate G_1 at this time generates displacement current onto D_2. As D_2's potential falls temporarily, G_4 can support current and charges are accumulated in the receiving well underneath G_7. The potential of G_7 falls in response to the received charge and this signal is sensed and fed back to the opposite channel's barrier gate, G_5.

In this procedure, the positive output packet is sensed and used to limit charge flow into the negative output, and vice versa. As more charge appears in one output, more charge is blocked from entering the opposite receiving well. Roughly speaking, common-mode signal appears as a common decrease in floating gate potentials and this quantity is fed back and subtracted from the outputs. At the same time, differential signal is amplified and stored in the receiving wells.

In addition to those benefits mentioned above, differential charge replication provides the following advantages over floating gate sensing. First, the floating gate's voltage swing and associated decrease in CCD storage well capacity are reduced. Second, precharge and signal sensing are performed in an autozeroed manner with respect to barriers underneath G_3 and G_4, so that operation is insensitive to absolute thresholds. Finally, the floating gate is clocked with voltage levels and timing that allow charge transfers at reduced clock voltage swings.

In addition to those methods described above, charge replicators may also be operated in a single-ended manner to nondestructively sense and copy a single input packet [6]. In this case, gate G_5 and transistor N_1 are eliminated and G_7 is connected to an unconditional CCD clock. Since this approach operates entirely in the charge domain, it offers improved linearity and reduced sensitivity to device thresholds and biasing over other methods of charge replication.

C. Charge Splitting Circuits

The present device uses the technique of charge splitting, shown in Fig. 6, to divide scaling packets in half. The configuration is similar to that of a simple CCD shift register with the addition of a field oxide barrier, originating in the first storage well, into the active channel region [7]. Although others are possible, this barrier placement was chosen to minimize the impact of leading edge effects on the characteristics of succeeding transfer gates.

Such charge splitting elements are easily incorporated into surrounding CCD registers because they are geometrically

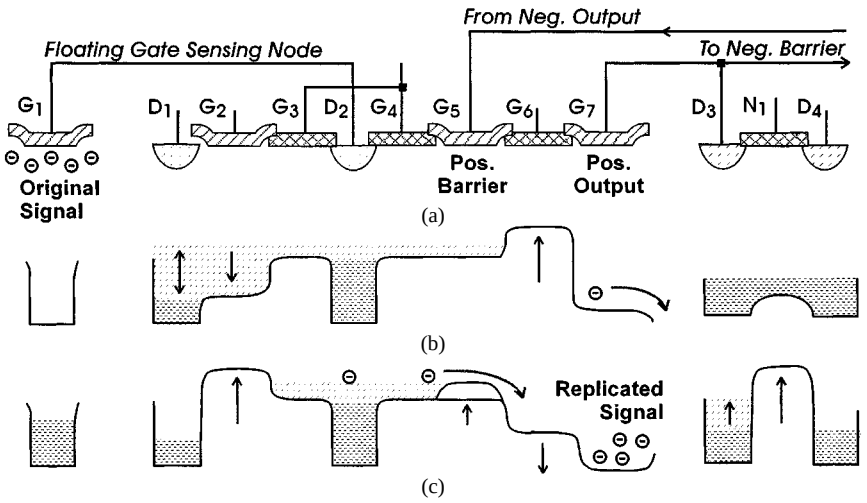


Fig. 5. Differential charge replicator. (a) Circuit configuration. (b) Precharge phase. (c) Sensing phase.

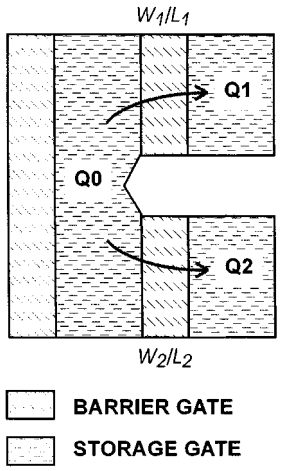


Fig. 6. Charge splitter configuration.

compatible and use identical clocking signals. Output packets are generated by integrating current through transfer gates with width-to-length ratios of W_1/L_1 and W_2/L_2 during the time that these gates are enabled. The conductance and charge that is integrated along each path forms a simple ratio

$$Q_1 = \frac{W_1 L_2}{W_2 L_1} Q_2. \tag{5}$$

A unique aspect of a charge-domain implementation is that charge conservation assures with extreme precision that

$$Q_1 + Q_2 = Q_0 \tag{6}$$

and that scaling channel errors are correlated between consecutive stages.

IV. Factors Limiting Conversion Accuracy

A. Propagating Errors

Errors that impact packets in the charge flow channels are referred to as propagating because they are passed on to, and accumulated in, subsequent pipeline blocks. Propagating errors result in permanent loss of information because they are indistinguishable from genuine signals. Charge splitting inaccuracy is a primary source of propagating error in the CDC. Systematic inaccuracy is caused by factors such as threshold nonuniformity, geometric mismatch, and nonuniform resistive delays in the charge splitting circuits. Dynamic errors are caused by uncertainty in the path of carriers in the vicinity of the splitting barrier.

The sign of a charge splitting error determines its impact on the converter's transfer characteristic. A larger than ideal scaling packet results in missing codes, while a larger than ideal accumulator packet results in missing decision levels [6]. To prevent missing codes or decision levels from appearing at the converter's output, the error, e, must satisfy

$$e[m]/g[m-1] < 2^{(-N-m+1)} \tag{7}$$

where N and m represent the number of conversion blocks and the error's position, respectively. Since splitting inaccuracies are primarily multiplicative in nature, and scaling signals decrease exponentially along the pipeline, this requirement is most appropriately expressed as a percentage of the total charge before the split. The most stringent requirements exist for earlier conversion blocks, where the signal to be split is larger.

As a result of (6), splitting errors cause discontinuities at subrange midpoints but do not alter subrange endpoints. For example, when the stages following a single error generate all "1's" or all "0's," the accumulator charges and, therefore the converter's result, are not impacted by the error.

B. Nonpropagating Errors

Errors that indirectly impact packets in the accumulator channels are referred to as nonpropagating because they are not passed forward to subsequent pipeline blocks. Nonpropagating errors do not result in permanent loss of information. For example, those that do not produce an incorrect comparison have no impact on the converter's output. Although not included in the present device, digital error correction could be used to compensate for errors that do cause an incorrect comparison [8].

TABLE I
PROTOTYPE DESIGN PARAMETERS

	CDC1	CDC2
OPTIMIZED FOR	RESOLUTION	POWER, SPEED
# CONVERSION BLOCKS	9	8
FULL-SCALE	500,000 e-	500,000 e-
COMPARATOR TYPE	ANALOG AMPLIFIER	DIGITAL FLIP-FLOP
FABRICATION TECHNOLOGY	CCD/CMOS	CMOS
CCD ELEMENT TYPE	BURIED CHANNEL	SURFACE CHANNEL
CCD CLOCKS	OFF CHIP	ON CHIP
CMOS CLOCKS	ON CHIP	ON CHIP
DESIGN RULES	2.0 μm	1.2 μm
ACTIVE DIE AREA	1.5 x 1.0 mm	0.8 x 0.6 mm

The primary sources of nonpropagating errors in the CDC are elements in the path from charge sensing through comparison. Linearity is not required from these circuits, provided their transfer characteristic remains monotonic, because nonlinearities will not alter the comparator's result. The present device makes use of differential charge replicators, with positive feedback and a highly nonlinear transfer characteristic, to implement this path.

Differential replication is subject to dynamic and static noise sources that are absent from depleted charge operations. These occur because a nondepleted source of carriers is necessary to implement nondestructive sensing. The primary sources of dynamic errors are thermal noise, introduced during both precharge and sensing, and coupled charge, added from nearby signal transitions. Static errors are caused by mismatches in replication efficiency between differential elements.

Each source of nonpropagating error produces both missing codes and missing decision levels in the converter's transfer characteristic [6]. Since signals in a charge-domain implementation are not amplified as they pass along the pipeline, requirements for the error, e, are most appropriately expressed as

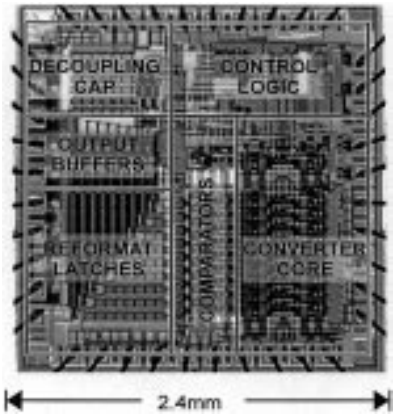
$$e[m]/g \leq 2^{-(N-1)} \tag{8}$$

where N, m, and g represent the number of conversion blocks, the position of the error, and the scaling input, respectively. The impact of nonpropagating errors is similar for all conversion blocks in the pipeline.

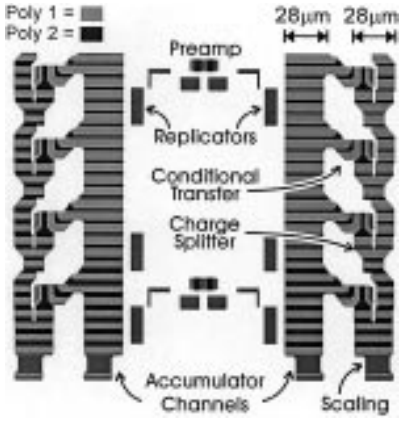
V. DEVICE MEASUREMENTS

Two prototype devices were built and tested. A summary of their design parameters is provided in Table I. The first prototype, referred to as the CDC1, includes nine conversion blocks. The focus of this device is on resolution, with no emphasis on optimizing its speed or power. Resolution is optimized in two ways. First, a CMOS preamplifier is included after charge sensing to improve comparator resolution. Second, the device is implemented in a CCD/CMOS process with 2.0-μm design rules that provides buried channel CCD's, improves charge transfer efficiency, and increases sensing speed.

Fig. 7(a) shows a chip photomicrograph of the CDC1. The converter core, control logic, and comparators occupy an area



(a)



(b)

Fig. 7. CDC1 prototype. (a) Chip photomicrograph. (b) Magnified CCD channel region.

of 2.6 mm^2. Fig. 7(b) shows a magnified view of active CCD channel regions in the converter core. The location and size of charge channels, splitters, and conditional transfer gates are indicated on the plot. Replicators and preamplifiers are located between the CCD channels, while the final comparison stage is located outside of this region. Storage gates on first level and barrier gates on second level polysilicon have lengths of 6.6 μm and 2.4 μm, respectively.

The second prototype, referred to as the CDC2, includes eight conversion blocks. Its focus is on high speed and low power, with little emphasis on optimizing its resolution. Power and speed are optimized in two ways. First, the device does not include any static circuits and utilizes simple digital flip-flops for performing comparison. Second, the device is implemented in a commercial CMOS process with smaller, 1.2 μm, design rules. This process does not include provisions for CCD's. As a result, all CCD circuits are implemented using surface channel elements and have reduced charge transfer accuracy and sensing speed.

Device measurements were performed using an automated A/D converter test bed. Performance of the two prototypes is summarized in Table II. To facilitate testing and characterization, both prototypes include an initial charge generation stage and are designed to accept voltage inputs. The CDC1 is controlled by means of four externally generated 5 V clocks

TABLE II
PROTOTYPE PERFORMANCE SUMMARY

	CDC1	CDC2
SPUR-FREE DYNAMIC RANGE	56 dB (at 2MHz)	49 dB (at 15MHz)
FACTOR LIMITING SFDR	CHARGE GENERATION	COMPARATORS
MAX SAMPLING RATE	5 MHz	22 MHz
FACTOR LIMITING MSPS	COMPARATORS	CONTROL LOGIC
POWER AT MAX RATE	20 mW	13 mW
% STATIC POWER	50	0
COMMON-MODE RESPONSE	1 LSB	--
CTE STEP RESPONSE	0 LSB	--
POWER SUPPLY	5 V	4 V

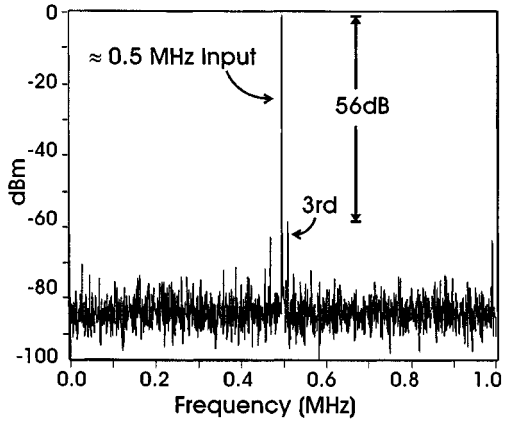
that are applied to the CCD gates. Barrier and storage signals are offset by 1 V. All CMOS controls are generated on-chip from these inputs. The CDC2 is controlled by means of four externally generated, 0 to 5 V clocks. All CCD and all CMOS clocks and controls are produced on-chip from these inputs. Differential and integral nonlinearity tests were not possible from the existing test setup.

Fig. 8(a) shows measured spectral response of the CDC1 with a 0.5 MHz sinusoidal input and a 2 MHz sampling rate. The signal-to-distortion ratio of 56 dB is limited by the third harmonic, which is attributed to the initial voltage-to-charge generation stage. The next largest harmonic is the ninth which lies at −63 dB. Fig. 8(b) shows the measured effective bits or signal-to-noise plus distortion, as a function of input power, under the same operating conditions. At its maximum sampling rate of 5 MHz, the CDC1 consumes 20 mW of power, 50% of which occurs in its CMOS preamplifiers and comparators.

The impact of comparator and charge splitting inaccuracies is inferred from the form of deviations in the converter's transfer characteristic from ideal. At frequencies up to 4 MHz, the two most significant sources of distortion are nonlinearity in the initial charge generation stage and imbalances between complementary sensing and preamplification circuits. Above 5 MHz, charge splitting errors, caused by increased resistive delays along the splitting gates, are an additional source of distortion. At this speed there is also an increase in the device's noise floor as a result of spurious codes, attributed to insufficient settling in the CMOS preamplifiers.

Charge transfer efficiency was evaluated by observing the CDC1's output from a full-scale step input. The impact of incomplete charge transfer was determined to be less than one LSB because no trailing signal was evident. Common-mode response was measured by observing the CDC1's output while identical full-scale ramps were applied to both the positive and negative inputs. One bit variation was observed in the output over this range.

Fig. 9 shows measured spectral response of the CDC2 device for a 0.5 MHz sinusoidal input and a 15 MHz sampling rate. The signal-to-distortion ratio is 49 dB. A slow input frequency is chosen to permit evaluation of converter performance without emphasis on surface channel charge transfer efficiency. At its maximum sampling rate of 22 MHz, the device consumes 13 mW of dynamic power and no static power. This measure includes power in the on-chip CCD



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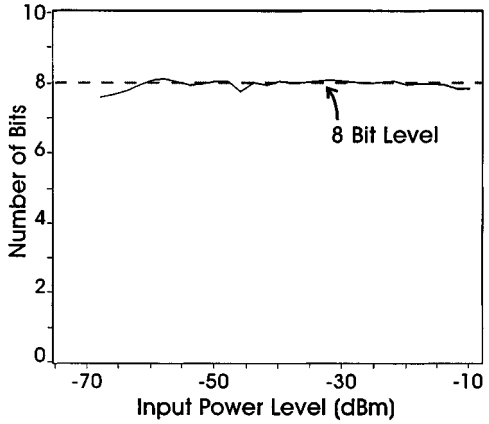

(b)

Fig. 8. CDC1 measurements for a 0.5 MHz input sinusoid and a 2 MHz sampling rate. (a) Spectral response. (b) Effective bits or SNDR.

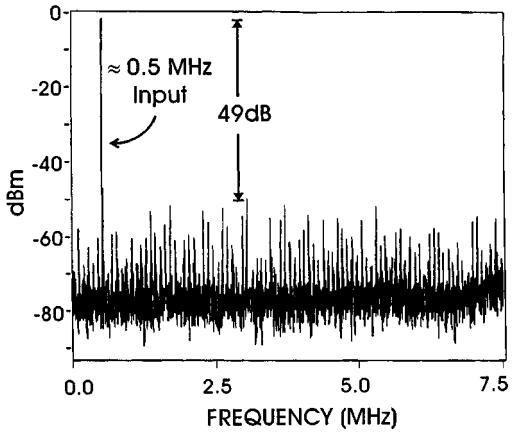

Fig. 9. CDC2 spectral response for a 0.5 MHz input sinusoid and a 15 MHz sampling rate.

clock generators. Coupling to the dynamic sensing nodes and inaccuracy in the flip-flop comparators limit the CDC2 resolution for frequencies up to 22 MHz. Performance is relatively constant over this range. Above this speed, performance degrades sharply as a result of control logic failure.

VI. CONCLUSION

Charge-to-digital conversion offers advantages over conventional charge readout techniques because it performs digitiza-

tion in the charge domain. A CDC architecture is described that uses operations, such as shifting, addition, and division, that are easily and accurately performed using CCD's. Duplicate scaling channels increase comparator symmetry and permit dynamic sensing circuits with feedback. New methods of generating charge provide improved linearity over conventional techniques. New methods of sensing charge and comparing charge packets improve comparator resolution by incorporating charge-domain differential amplification and common-mode suppression. Charge splitting error, comparator error, and charge transfer inefficiency are primary factors limiting converter resolution.

Measured results are presented for two prototype CDC's. The first, using buried channel CCD's, is optimized for resolution. It achieves 56 dB SFDR at a 2 MHz sampling rate and requires 20 mW at its maximum sampling rate of 5 MHz. The second, using surface channel CCD's, is optimized for power and speed. It achieves 49 dB SFDR at a 15 MHz sampling rate and consumes 13 mW power at its maximum sampling rate of 22 MHz.

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