A 200-MHz CMOS Phase-Locked Loop with Dual Phase Detectors

KURT M. WARE, MEMBER, IEEE, HAE-SEUNG LEE, MEMBER, IEEE, AND CHARLES G. SODINI, MEMBER, IEEE

Abstract—**A high-frequency integrated CMOS phase-locked loop (PLL) including two phase detectors is presented. The design integrates a voltage-controlled oscillator, a multiplying phase detector, a phase-frequency detector, and associated circuitry on a single die. The loop filter is external for flexibility and can be a simple passive circuit. A 2-μm CMOS p-well process was used to fabricate the circuit. The loop can lock on input frequencies in excess of 200 MHz with either or both detectors and consumes 500 mW from a single 5-V supply. The oscillator is a ring of three inverting amplifiers, and it draws power from an internal supply voltage regulated by an on-chip bandgap reference. This combination serves to reduce the supply and temperature sensitivities of the oscillator. The measured oscillator supply sensitivity is less than 5 percent/V; oscillator temperature variation is 2.2 percent in the range of 25 to 80°C. The typical oscillator tuning range is 112 to 209 MHz. The multiplying phase detector and phase-frequency detector (PFD) exhibit input-referred phase offsets of $< 4°$ and $-24°$, respectively. A numerical system simulation program was written to explore the time-domain behavior of an idealized model based on the phase-locked loop design.**

I. Introduction

THE COMMERCIAL success of local area networks and the demand for higher data rates have recently increased the need for inexpensive high-frequency phase-locked loops [1]. Data storage and RF data communications applications have also added to this need [2]. Silicon CMOS is a natural technology for these circuits because the high production volume of digital CMOS circuits has significantly reduced the unit cost. In addition, because many phase-locked loops are part of a larger CMOS digital or analog system, the potential for a higher level of integration exists in such applications [3].

Dual-loop phase-locked loops are an active topic of research, mostly due to the desire to improve the trade-off between acquisition behavior and locked behavior [4], [5]. In this paper, a 200-MHz CMOS phase-locked loop (PLL) incorporating a multiplying phase detector and phase-frequency detector is described. The loop filter is external for flexibility, and it may be a simple passive circuit. Either detector may be used by itself, or the two may be used together in certain applications.

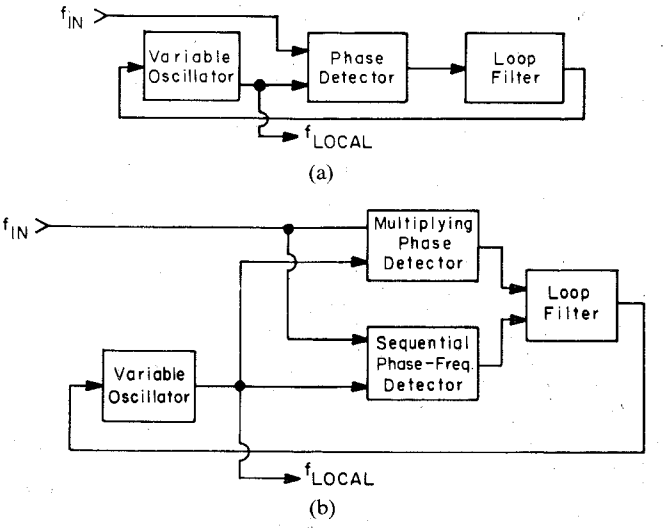


Fig. 1. (a) Single-loop PLL. (b) Dual-loop PLL.

Fig. 1(a) shows the block diagram of a conventional single-loop PLL, which contains a variable oscillator, phase detector, and loop filter. Fig. 1(b) shows the block diagram of a dual-loop PLL which makes use of a multiplying phase detector and a sequential phase-frequency detector.

There are two reasons to include both a phase detector and a frequency detector on the PLL integrated circuit. First, the appropriate type of detector is quite application dependent. For example, a PLL employing a multiplying phase detector is well suited to locking on a data pulse stream, whereas a PLL employing a phase-frequency detector (PFD) is well suited to frequency synthesis since the input signal does not have missing transitions [6], [7]. Second, frequency detection can be used to improve PLL signal acquisition. Consider a data synchronizer application where the PLL input is a pulse stream with packets of data separated by recognizable periods of 100 percent pulse density. The dual-loop PLL of Fig. 1(b) can be used as a fast acquisition data synchronizer. The PFD aids frequency acquisition because the multiplying phase detector provides insufficient frequency feedback when the loop

Manuscript received May 11, 1989; revised August 10, 1989. This work was supported by Analog Devices, AT&T, DEC, General Electric, IBM, and Texas Instruments Incorporated, and in part by DARPA under Contract N00014-87-K-0825.

K. M. Ware was with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139. He is now with the Jet Propulsion Laboratory, Pasadena, CA 91109.

H.-S. Lee and C. G. Sodini are with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139.

IEEE Log Number 8931197.

0018-9200/89/1200-1560$01.00 ©1989 IEEE

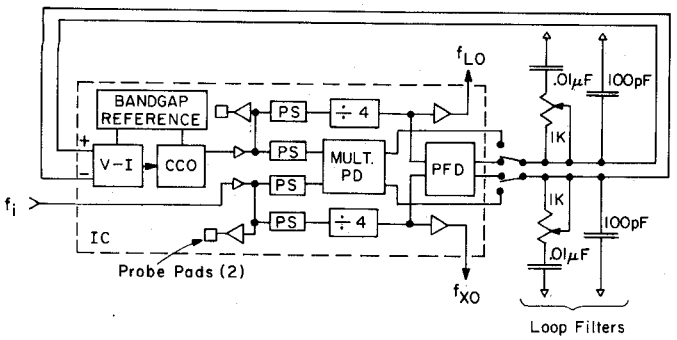


Fig. 2. Integrated circuit block diagram with example loop filter.

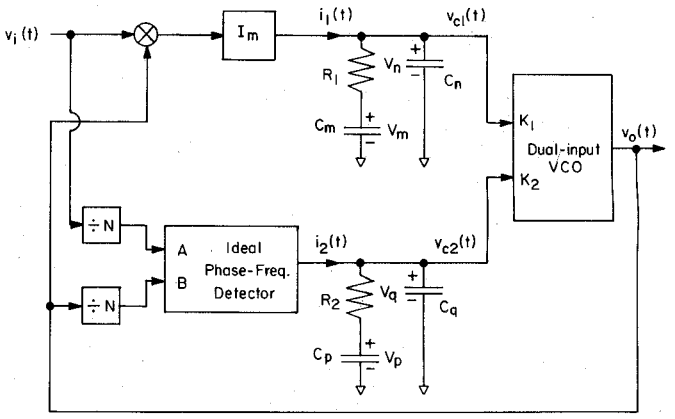


Fig. 3. Idealized model of a dual-loop PLL used for system simulator.

bandwidth is smaller than the input frequency difference [7]. Frequency detection must be enabled during the periods of 100-percent pulse density and disabled during the data packets.

Fig. 2 shows a block diagram of the integrated circuit and a simple passive loop filter connected to the PFD output. The variable oscillator consists of three parts: a voltage-to-current converter, a current-controlled oscillator, and a bandgap reference. The reference is used to reduce the supply and temperature sensitivity of the oscillator. Each block marked PS is a phase splitter, which generates a differential output to drive the multiplying phase detector and the frequency dividers. Frequency division by a factor of 4 allows the PFD to operate properly at the maximum oscillator frequency. Outputs f_{LO} and f_{XO} are taken from the dividers to drive external pins. Both the multiplying phase detector and the PFD generate differential output currents.

In this paper, Section II gives an overview of a simulation program used to explore the behavior of an idealized dual-loop phase-lock system based on the integrated circuit design. In Section III, the PLL circuits are described. Experimental results are presented in Section IV.

II. Numerical Simulation of the PLL

The response of a PLL to limited phase variations can be found by examining a linearized system model and using frequency-domain methods [7]. Due to its nonlinear behavior, the response to large phase variations cannot be found in a similar fashion. Some loops can be described by ordinary differential equations, which in nearly all cases must be integrated by computer for a particular input [8]. A loop employing a PFD cannot be described by a differential equation unless simplifying approximations are made [9].

For a particular input, the time-domain response of a PLL can be found with a circuit simulator such as SPICE [10]. However, simulating a PLL with many transistors is expensive, especially because the system is often characterized by widely spaced natural frequencies. For example, circuit simulation of a high-frequency narrow-band phase-lock system requires very small time steps to model the oscillator output, but the time scale of interest, such as the acquisition time, could be orders of magnitude larger than the time-step size. As a result, conventional circuit simulation of a complex PLL is impractical.

Simulation at the system level requires less computer time than circuit simulation because idealized models are used. Although some nonideal behavior is not modeled, system simulation retains the major characteristics of the actual system and allows one to explore design trade-offs [11]. A computer program was written to simulate the time-domain response of a restricted class of PLL's using idealized models for the loop components. The program can simulate the response of a loop employing the multiplying phase detector, the PFD, or both detectors. In the last case, numerical simulation is essential to assessing acquisition behavior.

Fig. 3 shows the system modeled by the simulator. The input signal model is $v_i(t) = \sin(\theta_i(t))$, and the output signal model is $v_o(t) = \sin(\theta_o(t))$. A constant I_m sets the magnitude of the multiplier output so $i_1(t) = I_m \cdot \sin(\theta_i(t)) \cdot \sin(\theta_o(t))$. The ideal PFD changes state only when the A and B inputs cross zero with positive slope, and its output current is $+I_p$, 0, or $-I_p$, depending on the state [9]. The voltage-controlled oscillator (VCO) output frequency is $\omega_o(t) = 2\pi f_c + K_1 v_{c1}(t) + K_2 v_{c2}(t)$, where f_c is the center frequency.

The oscillator output frequency $\omega_o(t)$ is integrated numerically using the first-order forward Euler method to find the output phase $\theta_o(t)$. The forward Euler method is used because other methods require an estimate of the control voltages at time t in order to compute their value at t. The nature of the PFD logic makes it difficult to use other integration methods because a small change in the estimate of the control voltages could cause the PFD model to change state and lead to a divergent solution. The time-step size is conservatively set to ensure that the natural frequencies of the discretized system fall in the stable region.

The time steps are chosen as follows. When the PFD logic enters a new state at time t_0, the current VCO and input frequencies are used to estimate the end time t_e of that state. The time-step size is set to $\Delta t = (t_e - t_0)/M$, where M corresponds to the target number of time steps per single-logic-state interval. The estimate for t_e is revised

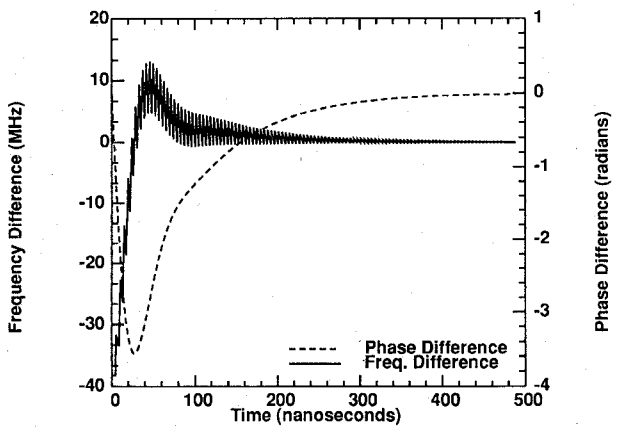


Fig. 4. Simulated step response of a PLL employing a PFD.

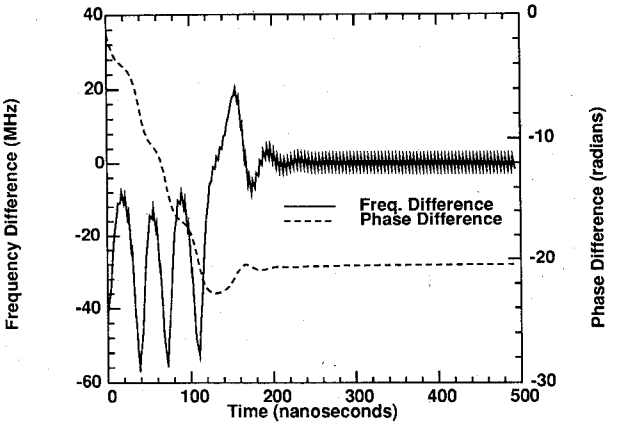


Fig. 5. Simulated step response of a PLL employing a multiplying phase detector.

for each time step. The last time step in the single-logic-state interval is sized to terminate on the most recent estimate of t_e. To assure reasonable accuracy, the value of M was adjusted until the actual number of time steps per interval was equal to the target number for a wide-band loop. Several wide-band loop simulations were carefully examined to assess the correctness of the method.

Capacitor voltages v_m, v_n, v_p, and v_q are treated as state variables. Because $i_2(t)$ is constant during the time step $(t_0,\ t_0+\Delta t)$, it is possible to exactly solve for $v_p(t_0+\Delta t)$ and $v_q(t_0+\Delta t)$. This calculation yields $v_{c2}(t_0+\Delta t)$.

During the time step, one can approximately solve for $v_{c1}(t_0+\Delta t)$. The current $i_1(t)$ is $I_m\cdot\sin(\theta_i(t))\cdot\sin(\theta_o(t))$. If one assumes that the time step is small enough to assure that $(\omega_i-\omega_o)\Delta t \ll 1$ and $(\omega_i+\omega_o)\Delta t \ll 1$, one can then substitute small-angle approximations for their sine and cosine. Under the approximation, we may solve for $v_m(t_0+\Delta t)$ and $v_n(t_0+\Delta t)$ in terms of their value at the beginning of the interval. This calculation yields $v_{c1}(t_0+\Delta t)$.

Loops employing only one of the phase detectors can be simulated by setting K_1 or K_2 to zero. In addition, because the loop filters are linear, the response of a system with two phase detectors connected to a single loop filter can be derived by superposition. If $R_1=R_2$, $C_m=C_p$, and $C_n=C_q$, the capacitor voltages in the single filter will be equal to the sum of the voltages on their counterparts in the system with two loop filters.

A sample of the simulator output is shown in Fig. 4. For this simulation, K_1 was set to zero to simulate the response of a loop employing the PFD alone. The input frequency was stepped at $t=0$ from 191 to 229 MHz. The frequency and phase difference plotted correspond to the difference between the input signal and the simulated oscillator output.

Loops employing only a multiplying phase detector were also simulated. If the initial frequency difference is large, the desired part of the multiplying phase detector output can lie outside the loop bandwidth, and it is attenuated. Acquisition in this case can be very slow or, if an offset is present in the loop, fail to occur entirely [7]. Fig. 5 shows the response of a loop employing the multiplying phase detector given an input frequency step at $t=0$ from 191 to 235 MHz. The cumulative phase difference decreases several cycles during acquisition and comes to a new equilibrium at a phase corresponding to -3.25 cycles.

The simulator duplicates the behavior predicted by linearized models where applicable and shows the expected nonlinear behavior. The simulator was used to efficiently explore the acquisition behavior of various single-loop and dual-loop systems.

III. Circuit Descriptions

In the following sections, the PLL subsystems will be described in more detail. In particular, the voltage-controlled oscillator, multiplying phase detector, and the phase-frequency detector circuits are presented.

A. Voltage-Controlled Oscillator

The voltage-controlled oscillator includes a voltage-to-current converter, a current-controlled ring oscillator, and a bandgap reference. The ring consists of three inverting amplifiers that combine an inverter in parallel with a current-controlled inverter. The inverter is a fast circuit that would make a high-frequency ring oscillator, whereas the current-controlled inverter permits the oscillator to be tuned over a suitable range. The supply and temperature sensitivities of this design are improved by using an internal reference.

Fig. 6 shows the current-controlled oscillator circuit. The node labeled V_{RR} is an internal supply voltage whose nominal value is 0.5 V. The ring oscillator includes $M1-M25$; $M26-M33$ constitute a voltage follower to set V_{RR} to the same voltage as the V_{REF} input. Devices $M1-M3$ control the oscillation frequency by setting the bias of the current-controlled inverters. The three inverting amplifiers in the ring are made up of devices $M4-M21$ whereas $M22-M24$ buffer the output signal. The first inverting amplifier in the ring consists of $M7$ and $M13$ (the inverter) and $M4$, $M8$, $M14$, and $M19$ (the current-controlled inverter).

Devices $M26-M33$ constitute a simple two-stage op-amp connected in a voltage-follower configuration. If vari-

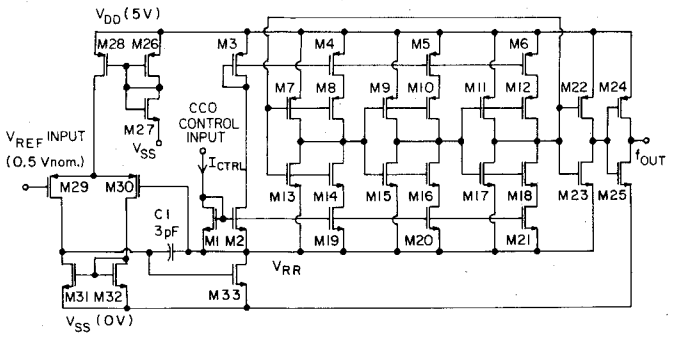


Fig. 6. High-frequency ring-oscillator schematic.

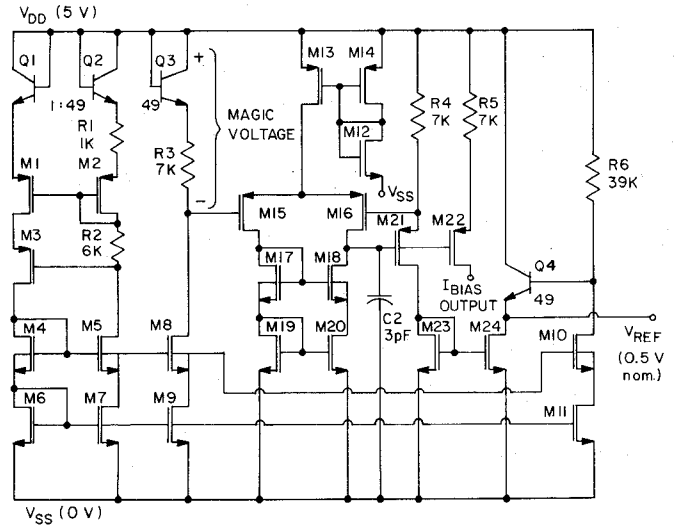


Fig. 7. Bandgap current source and voltage reference schematic.

ations in V_{DD} are duplicated exactly by V_{REF}, $V_{DD}-V_{RR}$ is constant, and the ring-oscillator supply sensitivity to V_{DD} will be greatly reduced. This design was fabricated using a p-well process; by tying the wells of $M13-M21$ to their respective source terminals, the oscillator is nearly isolated from substrate voltage variations.

The op amp uses $M33$ for the second stage; its width is large to assure the device remains saturated when its drain-to-source voltage is 0.5 V. Pole-splitting compensation is performed by $C1$, which is a sandwich of metal-2, metal-1, and p-well material. Simulations indicated that $C1$ improves the op-amp open-loop phase margin to 79°.

The center frequency temperature sensitivity of the uncompensated oscillator was measured at -2000 ppm/°C. The voltage-follower input V_{REF} has a nominal value of -4.5 V, referred to V_{DD}, on which an intentional temperature coefficient (TC) of $+2400$ ppm/°C is induced. Through the oscillator center frequency sensitivity to V_{RR}, the ring-oscillator temperature sensitivity is greatly reduced.

The reference voltage V_{REF} is generated on-chip by the circuit in Fig. 7. This circuit is an adaptation of a basic CMOS bandgap current source [12], and it also generates a bias current I_{BIAS} used in the voltage-to-current converter. Devices $Q1$, $Q2$, $R1$, $R2$, and $M1-M11$ serve to generate bias voltages across $R3$ and $R6$, which are proportional to absolute temperature (PTAT). Devices $M12-M20$ form an op amp that sets the voltages across $R4$ and $R5$ equal to the magic voltage across $Q3$ and $R3$, and $M21$ and $M22$ act as source followers. The op amp is compensated by $C2$, which improves the op-amp open-loop phase margin to 72° according to simulation. A temperature-independent current is mirrored by $M23$ and $M24$ through the emitter of $Q4$, which, with $R6$, creates the V_{REF} output.

The n-p-n transistors here are substrate–well–n^+ devices that are available in any p-well CMOS process. The collector terminals of all such devices are connected through the substrate to V_{DD}. Transistor $Q1$ is constructed with a single 10-μm square emitter; $Q2-Q4$ have 49 such emitters in parallel.

Ordinarily, the place of $R2$ would be taken by a diode-connected p-channel transistor, and the circuit would require a supply voltage greater than 5 V. With $R2$, $|V_{DS}|$ of $M1$ is reduced, and the circuit can operate from 5 V with standard threshold transistors.

All resistors shown are made from polysilicon material. The magic voltage across $Q3$ and $R3$ is designed to exhibit a TC equal to that of resistors $R4$ and $R5$ to make the I_{BIAS} output current (250-μA nominal) supply and temperature independent. The voltage $V_{DD}-V_{REF}$ has a nominal value of 4.5 V along with a temperature coefficient of

$$\mathrm{TC}_{V_{REF}} = \frac{3.9\ \mathrm{V}}{4.5\ \mathrm{V}} \cdot \frac{1}{T} + \frac{-2.3\ \mathrm{mV}}{4.5\ \mathrm{V}} \qquad (1)$$

or $+2400$ ppm/°C at room temperature.

Since the loop filter output is a control voltage, and the circuit of Fig. 6 is tuned by a current, a voltage-to-current converter is required. The differential control voltage is converted to a single-ended current output by a differential stage whose transconductance is largely determined by a polysilicon resistor. When the input differential voltage is zero, the output current is set by I_{BIAS}. The output current varies in a nearly linear fashion from zero to full scale for differential inputs from approximately -1.25 to $+1.25$ V.

SPICE simulation of the voltage-controlled oscillator using early device models indicated that the oscillator tuning range would be 170 to 270 MHz and that the transfer coefficient of the oscillator would be 15 MHz/V near the center frequency.

B. Multiplying Phase Detector

Practical multiplying phase detectors fall into three groups: linear [13], chopping [6], [14], [15], and EXCLUSIVE-OR [16]. The chopping multiplier and EXCLUSIVE-OR circuit generate a signal whose low-frequency components approximate those of the linear multiplier, but their high-frequency components will differ. In phase-lock applications, the loop filter attenuation tends to minimize the effect of these differences. Linear multipliers are often based on the double-balanced Gilbert cell [17]. The chopping multiplier can be based on a single-balanced Gilbert

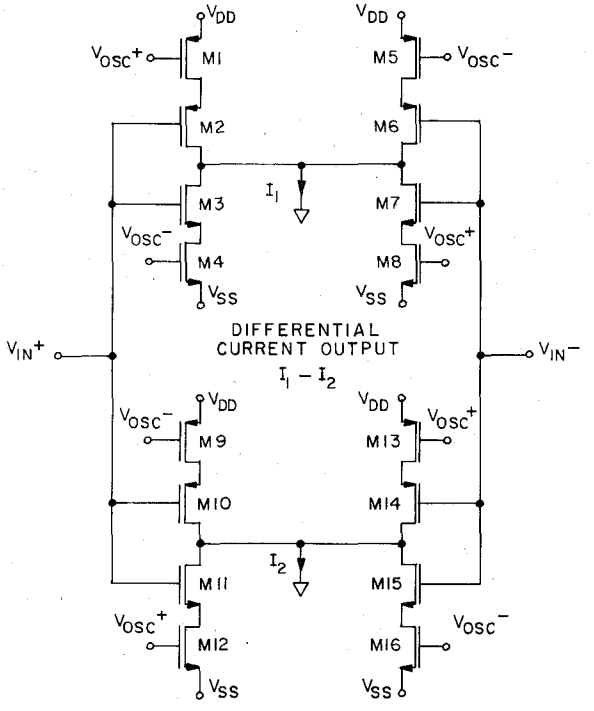


Fig. 8. Multiplying phase detector schematic.

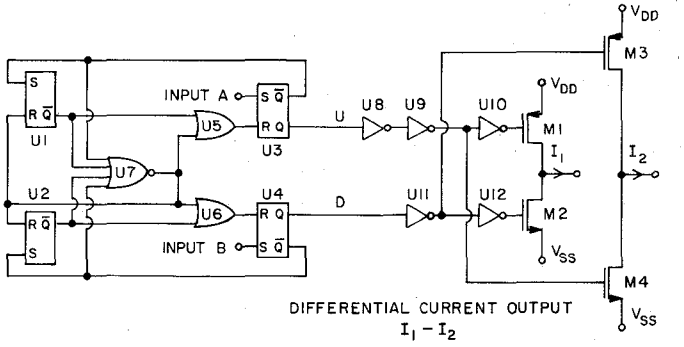


Fig. 9. PFD block diagram.

cell [6], [14] or switching between $+1$ and -1 amplifiers [15]. In the latter case, one may replace the amplifiers with a phase-splitter circuit, which generates differential outputs from a single-ended input.

In this work, a differential-output chopping multiplier was implemented. Fig. 8 shows the multiplying phase detector design. The differential signals V_{OSC+} and V_{OSC-} are generated from the VCO output by a phase splitter. Another phase splitter generates V_{IN+} and V_{IN-} from the PLL input signal. Transistors $M1-M8$ form one chopping multiplier and use tri-state gates to alternately switch the V_{IN+} and V_{IN-} signals to the output. When V_{OSC} is low, the tri-state inverter consisting of $M1-M4$ is enabled, whereas the inverter consisting of $M5-M8$ goes into high-impedance mode. When V_{OSC} is high, their roles are interchanged. If the output were unloaded, the resulting output voltage would correspond to the EXCLUSIVE-OR function of its inputs. Tying the output to incremental ground creates a current-mode output representing the product of the local oscillator output and the PLL input signal. Devices $M9-M16$ are the same as $M1-M8$ but are switched on the opposite phase of V_{OSC}.

The average output of an ideal multiplier is zero when the inputs are sinusoids of the same frequency and $\pm 90°$ out of phase. If we consider phase differences near $-90°$, an actual multiplying phase detector will have zero average output at a phase that is offset slightly. This offset between the ideal model and the actual circuit is the input-referred phase offset. The differential configuration in Fig. 8 is intended to reduce the input-referred phase offset.

Let us concentrate on one output I_1. If the input phase difference is $-90°$ and the load is purely capacitive, the output voltage will not settle at the midpoint between V_{DD} and V_{SS}; it will be at some voltage V_{DC} due to the difference in average current output between the n- and p-channel devices. Because the matching circuit, including devices $M9-M16$, is switched on the opposite phase, its output voltage should also be V_{DC}. The differential output voltage should be zero in this case and therefore be free of offset.

Supply voltage variations can cause some change in the magnitude of the phase characteristic but should not increase the input-referred phase offset because such variations will not affect the switching duty cycle.

If the V_{IN} and V_{OSC} signals do not have 50-percent duty cycle, a phase detector offset will result. The phase-splitter output signals are designed to have nearly 50-percent duty cycle at high frequencies so the phase detector offset is relatively small.

C. Phase-Frequency Detector

The phase-frequency detector in this work is based on the conventional design, with an edge-sensitive state machine controlling an output charge pump [9]. For compatibility with the multiplying phase detector design, a differential output circuit was designed. A block diagram of the phase-frequency detector design is shown in Fig. 9.

If the leading edge of input A precedes the leading edge of input B, $U1-U7$ will generate a pulse on U whose width corresponds to the time difference between the two leading edges. This pulse turns on $M1$ and $M4$, and the output differential current is then positive. Conversely, if the leading edge of B precedes A, a pulse appears on D, which turns on $M2$ and $M3$, generating a negative differential output current.

The maximum input frequency of the phase-frequency detector is significantly lower than the maximum oscillator output frequency. If the PLL input signal does not have missing or extra transitions, one may precede the PFD inputs with two identical frequency dividers. Since the PFD itself is intolerant of missing or extra transitions, this was not considered to be a restriction.

In this work, the frequency dividers preceding the PFD each consist of a cascade of two high-speed toggle flip-flops. The toggle flip-flop design is shown in Fig. 10. This is an adaptation of a GaAs design whose reported maximum toggle rate corresponds to $1/(2\tau_p)$, where τ_p is the gate propagation delay [18]. The input clocks CLK+ and

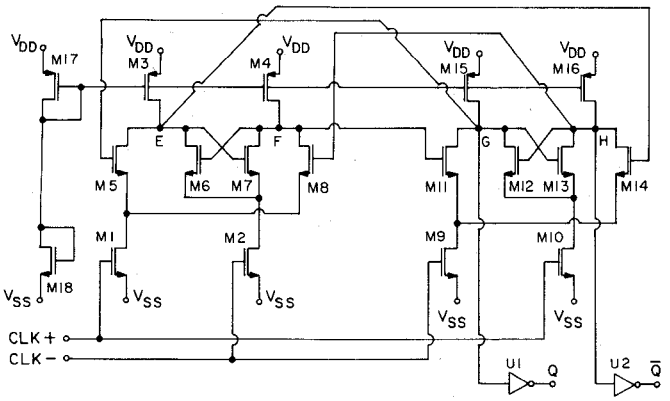


Fig. 10. Toggle flip-flop schematic.

CLK− are driven by a phase splitter or a previous divider stage, so they are complementary and have a nominal duty cycle of 50 percent. This is a differential master–slave configuration. The gates of $M5$ and $M8$ constitute the differential D and $\overline{D}$ inputs to the master flip-flop stage. When CLK+ is high, $M5$ and $M8$ transfer the input state to nodes E and F. When CLK+ goes low and CLK− goes high, the master state is held by a regenerative pair $M6$ and $M7$. Nodes E and F drive the slave stage, which is identical but switched on the opposite clock phases. The ON times of $M1$ and $M2$ overlap, as do those of $M9$ and $M10$, so the state is smoothly transferred from master to slave. Nodes G and H are the slave stage outputs. Node G is connected to the D input, and node H is connected to the $\overline{D}$ input; a logical inversion occurs between the slave stage output and the master stage input. This makes the circuit act as a toggle flip-flop. Inverters $U1$ and $U2$ serve to buffer the output and restore it to full voltage swing. The maximum input frequency of the divider exceeds the maximum frequency of the oscillator.

IV. Experimental Results

The prototype circuit was fabricated by MOSIS using their scalable CMOS 2-μm p-well process [19]. The process has two levels of metal interconnect and a nominal oxide thickness of 400 Å. A labeled photograph of the die is shown in Fig. 11. Each prototype circuit includes two complete PLL's, a VCO test circuit, and a bandgap reference test circuit. Major subsystems are labeled on the left-hand PLL in Fig. 11. The active area of the PLL with both detectors is 1.5×3.7 mm^2. The measured data presented in this section were taken from devices fabricated on two separate MOSIS runs sent to the same foundry.

A minor error was found in the bandgap reference design. To test the circuits as received, the oscillator temperature and supply sensitivities were measured with $V_{DD} = 6.0$ V. In this case, $V_{DD} - V_{REF}$ was close to the nominal value of 4.5 V. Because the oscillator frequency is primarily dependent on $V_{DD} - V_{REF}$ and much less dependent on $V_{REF} - V_{SS}$, these measurements should reflect the true circuit performance. All other measurements presented here were conducted with the nominal supply $V_{DD} = 5.0$ V.

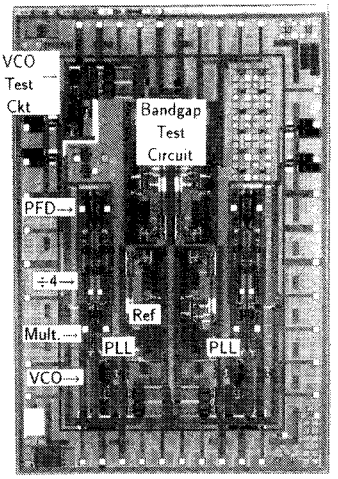


Fig. 11. Die photograph of the prototype PLL and test circuits.

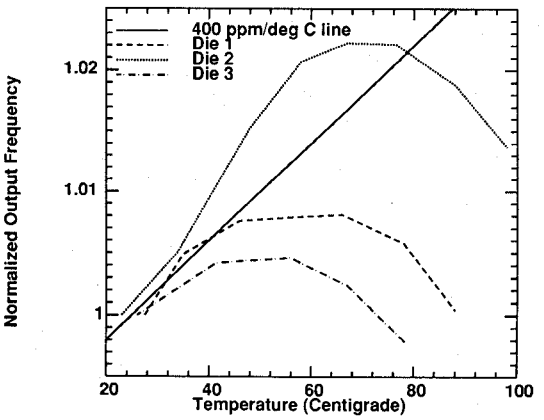


Fig. 12. Normalized oscillator temperature measurements.

The mean oscillator center frequency was measured at 190 MHz. Chip-to-chip center frequency variations of 148 to 234 MHz (±23 percent) were observed. The tuning range of a typical device was 112 to 209 MHz, which represents a reach of ±30 percent about the midpoint of the range. Although the center frequency varied widely from chip to chip, the oscillator range as a percentage of the center frequency was quite uniform. Out of 19 prototypes, 85 percent of the devices could reach frequencies from 128 to 187 MHz. All of the devices could reach 140 to 162 MHz, so the tuning range was deemed adequate to allow for chip-to-chip variation.

The worst-case supply sensitivity of the oscillator with the on-chip reference was measured at 4.7 percent/V, which is a fourfold improvement over the measured sensitivity when no on-chip reference was used. Fig. 12 shows the measured temperature dependence for three oscillators, along with a 400 ppm/°C line for comparison. The worst-case oscillator temperature variation was restricted to a 2.2-percent range for temperatures between 25 and 80°C, equivalent to an average temperature coefficient of 400 ppm/°C. This is a considerable improvement over the −2000 ppm/°C temperature coefficient of the uncompensated oscillator.

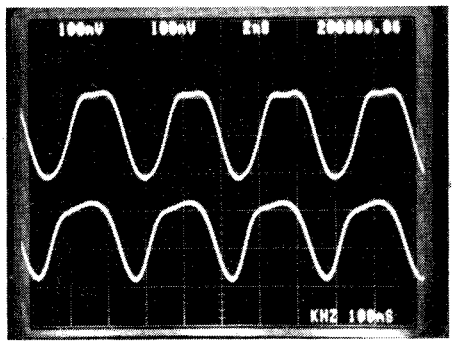


Fig. 13. PLL internal waveforms, locked on 200-MHz input, using the PFD. Top trace: buffered input signal. Bottom trace: buffered oscillator output. Vertical scale is 2 V/div; horizontal scale is 2 ns/div.

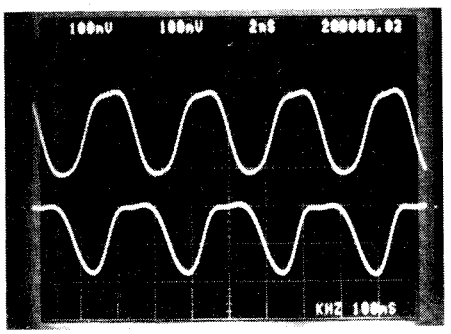


Fig. 14. PLL internal waveforms, locked on 200-MHz input, using the multiplying phase detector. Top trace: buffered input signal. Bottom trace: buffered oscillator output. Vertical scale is 2 V/div; horizontal scale is 2 ns/div.

When employing the phase-frequency detector, the PLL can lock on a 200-MHz sine wave, as shown in Fig. 13. The PLL input signal was amplified and limited by the input buffer circuit. These waveforms were measured on the chip at buffered probe pads, representing the PLL input signal and the oscillator output (see Fig. 2). A low-capacitance active probe was used to measure the signals, attenuating them by a factor of 20. The loop bandwidth was estimated to be 500 kHz. The loop can lock on input frequencies corresponding to most of the oscillator range. Pull-in occurs spontaneously over the entire lock range. This photograph shows a steady-state phase difference near 0°, as expected. Steady-state phase error measurements indicated that the input-referred phase offset of the PFD was $-6°$ at its input. This corresponds to a $-24°$ offset at the input of the frequency dividers, which contribute negligible phase offset.

When employing the multiplying phase detector, the PLL can lock on a 200-MHz sine wave, as shown in Fig. 14. The PLL input signal was amplified and limited by the input buffer circuit. These waveforms were measured on the chip at buffered probe points, representing the PLL input signal and the oscillator output. The loop bandwidth was estimated to be 1 MHz. The loop can lock on input frequencies corresponding to most of the oscillator range. The pull-in range varies, depending on the loop filter, but can correspond to most of the lock range. This photograph shows a steady-state phase difference near $-90°$, as expected. Steady-state phase error measurements indicated

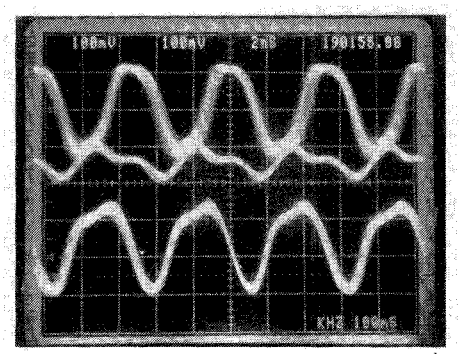


Fig. 15. PLL eye diagram, locked on 190-Mbit/s RZ data pulse stream input, using the multiplying phase detector. Top trace: buffered input signal. Bottom trace: buffered oscillator output. Vertical scale is 2 V/div; horizontal scale is 2 ns/div.

that the input-referred phase offset of the multiplying phase detector was less than 4°.

When employing the multiplying phase detector, the PLL can also lock on a data pulse stream. Fig. 15 shows an eye diagram, where the PLL input was a 190-Mbit/s repeating 64-bit return-to-zero (RZ) data pulse stream, and the oscilloscope was triggered on the trailing edge of the oscillator output. Due to the sizable eye opening, a decision circuit strobed by the oscillator could reliably regenerate the incoming data. An external delay was adjusted to place the trailing edge of the oscillator output in the center of the eye. The loop bandwidth was estimated to be 600 kHz.

The detector outputs are compatible and can be connected together directly. We note that the nominal steady-state input phase difference for the PLL employing the multiplying phase detector alone is $-90°$ compared with 0° when the PFD alone is used. When the two are used in combination, the phase characteristic is a composite, and the steady-state input phase difference lies between -90 and 0°. For this integrated circuit, the nominal steady-state phase difference is $-81°$; the frequency dividers preceding the PFD serve to reduce the effect of the PFD on the input phase difference. Measurements of the closed-loop behavior in this case were consistent with the composite phase characteristic model.

To demonstrate the applicability of the PLL with dual detectors, a prototype fast acquisition data synchronizer test circuit was designed and fabricated. A block diagram of the chip is shown in Fig. 16. The chip was designed to regenerate non-return-to-zero (NRZ) data, which is converted on chip to a RZ data pulse stream suitable for synchronization by the PLL. A half-bit delay and an EXCLUSIVE-OR circuit were used to implement the NRZ-to-RZ converter.

The carrier detector controls the PFD charge pump so that frequency detection is enabled during periods when the PLL input has 100-percent pulse density and disabled when the PLL input pulse density is less than 100 percent. The carrier detector employs a leading edge detector, a retriggerable one shot whose time constant determines the expected data rate, and a state register that keeps a record of the previous nine ZERO-to-ONE transitions. A logic cir-

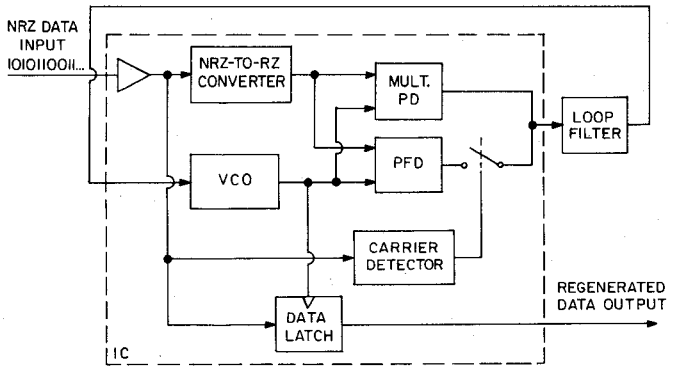


Fig. 16. Fast acquisition data synchronizer block diagram.

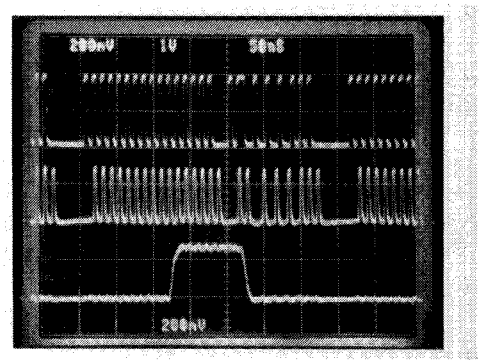


Fig. 17. Carrier detector measured waveforms. Top trace: NRZ data stream input, 1 V/div. Middle trace: edge detector output (internal), 4 V/div. Bottom trace: carrier detector output (internal), 4 V/div. Horizontal scale is 50 ns/div.

cuit generates the CD output. When an 18-bit 101010 $\cdots$ pattern is detected, the CD output goes high and stays high until the first ZERO-to-ONE transition after the pattern is broken and data are present.

The system shown in Fig. 16 is superior to one in which the CD output is used to independently multiplex the phase detectors. Because each phase detector results in a different steady-state input phase difference, a phase difference transient will result when the CD output changes. In the first case, the multiplying phase detector is always enabled, and the input steady-state phase difference is $-81°$ when the PFD is enabled and $-90°$ when the PFD is disabled. In the second case, the input steady-state phase difference is $0°$ when the PFD is used alone and $-90°$ when the multiplying phase detector is used alone. Thus, the shift in the phase difference required in the first case is much smaller than the second case—the system shown in Fig. 16 is superior. The details of the transient and its effect on the system performance will depend on the loop filter parameters and the application requirements.

The complete data synchronizer test circuit could not be tested due to a layout error. However, subsystem tests indicated the feasibility of the basic concept. Fig. 17 shows measured carrier detector waveforms with an NRZ input data rate of 180 Mbits/s. The CD output rising edge follows an 18-bit 101010 $\cdots$ pattern; the falling edge follows the first ZERO-to-ONE transition that does not match the minimum spacing.

TABLE I
SUMMARY OF MEASUREMENTS ON THE PHASE-LOCKED LOOP

VCO Mean Center Frequency	190 MHz
VCO Center Frequency Variation (Worst Case)	148 to 234 MHz ($\pm$ 23%)
VCO Tuning Range (Typical)	112 to 209 MHz ($\pm$ 30%)
VCO Transfer Coefficient	40 MHz/V
VCO Supply Sensitivity	4.7 %/V (max.)
VCO Temperature Variation	2.2% (max.) 25°C and 80°C 400 ppm/°C avg.
PFD Transfer Coefficient	370 μA/radian
PFD Input Referred Phase Offset	$-24°$
Mult. PD Transfer Coefficient	640 μA/radian
Mult. PD Input Referred Phase Offset	$< 4°$
PLL Supply Voltage	5 V
PLL Power Consumption	500 mW
PLL Active Area	1.5 mm $\times$ 3.7 mm

V. SUMMARY

A 200-MHz phase-locked loop with a multiplying phase detector and a phase-frequency detector has been constructed using a 2-μm CMOS process. An on-chip bandgap reference has been used to significantly improve the VCO supply and temperature sensitivities. The presence of dual phase detectors increases the application flexibility of the circuit, and some applications may benefit from the use of both phase and frequency detection. The entire PLL circuit operates from a single 5-V supply and consumes 500 mW when locked on an input at 200 MHz while driving two 50-Ω outputs at 50 MHz. A summary of the measured data is given in Table I.

ACKNOWLEDGMENT

The authors wish to thank J. K. Roberge for his suggestions regarding chip testing and P. Ferguson at Analog Devices, Inc. for providing access to apparatus for modifying test devices. They also wish to express their gratitude to MOSIS for fabricating the devices.

REFERENCES

[1] R. H. Leonowich and J. M. Steininger, "A 45-MHz CMOS phase/frequency-locked loop timing recovery circuit," in *ISSCC Dig. Tech. Papers*, 1988, pp. 14–15.
[2] W. D. Llewellyn, M. M. H. Wong, G. W. Tietz, and P. A. Tucci, "A 33 Mb/s data synchronizing phase-locked loop circuit," in *ISSCC Dig. Tech. Papers*, 1988, pp. 12–13.
[3] D. A. Hodges, P. R. Gray, and R. W. Broderson, "Potential of MOS technology for analog integrated circuits," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 285–294, June 1978.
[4] J. Scott *et al.*, "A 16 Mb/s data detector and timing recovery circuit for token ring LAN," in *ISSCC Dig. Tech. Papers*, 1989, pp. 150–151.
[5] J. D. Blair *et al.*, "A 16 MBPS adapter chip for the token-ring local area network," in *ISSCC Dig. Tech. Papers*, 1989, pp. 154–155.
[6] R. R. Cordell, J. B. Forney, C. N. Dunn, and W. G. Garrett, "A 50 MHz phase- and frequency-locked loop," *IEEE J. Solid-State Circuits*, vol. SC-14, pp. 1003–1009, Dec. 1979.
[7] F. M. Gardner, *Phaselock Techniques*, 2nd ed. New York: Wiley, 1979.
[8] A. J. Viterbi, *Principles of Coherent Communication*. New York: McGraw-Hill, 1966, ch. 3.
[9] F. M. Gardner, "Charge-pump phase-lock loops," *IEEE Trans. Commun.*, vol. COM-28, pp. 1849–1858, Nov. 1980.
[10] T. Quarles, A. R. Newton, D. O. Pederson, and A. Sangiovanni-Vincentelli, *SPICE 3B1 User's Guide*, Univ. of California, Berkeley, Apr. 1987.

[11] S. Can and Y. E. Sahinkaya, "Modeling and simulation of an analog charge-pump phase locked loop," *Simulation*, vol. 50, pp. 155–160, Apr. 1988.
[12] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 2nd ed. New York: Wiley, 1984, pp. 736–737.
[13] E. N. Murthi, "A monolithic phase-locked loop with post detection processor," *IEEE J. Solid-State Circuits*, vol. SC-14, pp. 155–161, Feb. 1979.
[14] M. Soyuer and R. G. Meyer, "A 350 MHz bipolar monolithic phase-locked loop," in *Proc. CICC*, 1988, pp. 9.6.1–4.
[15] B. J. Hosticka, W. Brockherde, U. Kleine, and R. Schweer, "Nonlinear analog switched-capacitor circuits," in *IEEE Int. Symp. Circuits Syst.*, 1982, pp. 729–732.
[16] C. S. Park and R. Schaumann, "Design of a 4-MHz analog integrated CMOS transconductance-*C* bandpass filter," *IEEE J. Solid-State Circuits*, vol. 23, pp. 987–996, Aug. 1988.
[17] B. Gilbert, "A precise four-quadrant multiplier with subnanosecond response," *IEEE J. Solid-State Circuits*, vol. SC-3, pp. 365–373, Dec. 1968.
[18] C. A. Liechti *et al.*, "A GaAs MSI word generator operating at 5 Gbit/s data rate," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-30, pp. 998–1006, July 1982.
[19] C. Tomovich, "MOSIS—A gateway to silicon," *IEEE Circuits Dev. Mag.*, vol. 4, pp. 22–23, Mar. 1988.

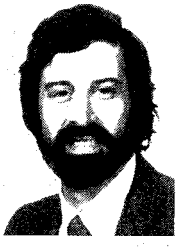
Kurt M. Ware (S'82–M'84) was born in Freeport, IL, in 1960. He received the B.S., M.S., and Ph.D. degrees from the Massachusetts Institute of Technology, Cambridge, in 1982, 1985, and 1989, respectively, all in electrical engineering.

In 1982 and 1983 he was with ADC Telecommunications, Edina, MN, where he was involved in circuit design for communications equipment. He is currently a member of the technical staff at the Jet Propulsion Laboratory, Pasadena, CA. His interests include analog and digital integrated circuits, phase-lock systems, and numerical simulation.

Hae-Seung Lee (M'85) was born in Seoul, Korea, in 1955. He received the B.S. and M.S. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 1978 and 1980, respectively. He received the Ph.D. degree in 1984 from the University of California, Berkeley.

In 1980 he was a Member of the Technical Staff in the Department of Mechanical Engineering at the Korean Institute of Science and Technology, where he was involved in the development of electromechanical systems. In 1984 he joined the faculty of the Massachusetts Institute of Technology, Cambridge, where he is now an Associate Professor. Since 1985 he has acted as a consultant to Analog Devices Semiconductor and Lincoln Laboratory. His research interests include CMOS and BiCMOS integrated circuits, IC fabrication technologies, and solid-state sensors.

Dr. Lee is a recipient of the 1988 Presidential Young Investigator's Award.



Charles G. Sodini (S'80–M'82) was born in Pittsburgh, PA, in 1952. He received the B.S.E.E. degree from Purdue University, Lafayette, IN, in 1974 and the M.S.E.E. and Ph.D. degrees from the University of California, Berkeley, in 1981 and 1982, respectively.

He was a member of the technical staff at Hewlett-Packard Laboratories from 1974 to 1982, where he worked on the design of MOS memory and later on the development of MOS devices with very-thin-gate dielectrics. He joined the faculty of the Massachusetts Institute of Technology (M.I.T.), Cambridge, in 1983, where he is currently an Associate Professor in the Department of Electrical Engineering and Computer Science. His research interests are focused on IC fabrication, device modeling, and device-level circuit design, with emphasis on analog and memory circuits.

Dr. Sodini held the Analog Devices Career Development Professorship of M.I.T.'s Department of Electrical Engineering and was awarded the IBM Faculty Development Award from 1985 to 1987. He has served on a variety of IEEE Conference Committees including the International Electron Devices Meeting of which he was the 1989 General Chairman.