A High-Swing 2-V CMOS Operational Amplifier with Replica-Amp Gain Enhancement

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***Abstract*— A general gain-enhancement technique for operational amplifiers using a replica amplifier is described. Unlike conventional techniques such as cascoding, which increases the gain by increasing the output resistance, the replica-amp technique increases the gain by matching the main and the replica amps. Among the advantages of the replica-amp technique are low supply, high swing, and effectiveness with resistive loads. This technique has been demonstrated in a 1.2-μm CMOS two-stage op amp. Operating from ± 1-V supplies, the op amp has an effective open-loop dc gain of greater than 10 000, while maintaining a high swing of 100 mV from either supply rails. The gain-enhancement circuit is shown to have only a small effect on the settling time experimentally, analytically, and in SPICE simulation.**

I. Introduction

PORTABLE systems are currently moving from 5-V to 3.3-V supplies, with a trend toward even lower supply voltages. At these low supply voltages, the design of analog circuits is extremely challenging. The key bottleneck is the operational amplifier, which typically requires high open-loop gain and high-frequency response to minimize errors in the output voltage, and high output swing to maximize the signal-to-noise ratio, especially in low-supply applications. Obtaining high open-loop gain, however, is difficult in modern MOS processes due to the small intrinsic gain of short-channel MOS transistors. Although long-channel transistors or subthreshold operations improve gain, the frequency response is sacrificed. A number of circuit techniques have been used to increase the gain by increasing the output resistance. Fig. 1(a) shows a simplified version of the popular cascode. The output resistance is increased by a factor of $g_m r_o$, so the voltage gain is increased by the same factor [1]. This increase in gain, however, is achieved at the expense of the output swing. Although 1 $V_{DS,\mathrm{SAT}}$ is necessary to saturate the bottom transistor, typically a safety margin V_{margin} is added to ensure that the bottom transistor operates in the saturation region. Taking into account the additional 1 $V_{DS,\mathrm{SAT}}$ for the top transistor, the maximum swing from supply is 2 $V_{DS,\mathrm{SAT}} + V_{\mathrm{margin}}$. Since both $V_{DS,\mathrm{SAT}}$ and V_{margin} are on the order of 200 mV, the sacrifice in output swing can be very large, especially in low-supply circuits. Fig. 1(b) shows the active cascode circuit [2], [3]. By adding an additional amplifier, the output resistance is increased by the additional gain of A. Since the circuit requires a regular cascode, it suffers the same output-swing limitation of 2 $V_{DS,\mathrm{SAT}} + V_{\mathrm{margin}}$. A number of circuits using positive feedback to bootstrap the output resistance have been reported [4]–[6]. Fig. 1(c) shows an example from [4]. It can be shown that in the worst case, the gain enhancement is turned off when the output swings within 2 $V_{DS,\mathrm{SAT}} + V_{\mathrm{margin}} + V_T$ from the supply. This limitation is quite severe since V_T is typically on the order of 700 mV. Although other positive feedback circuits such as [7] may not suffer as severe an output-swing limitation, in most cases the output swing is limited to 2 $V_{DS,\mathrm{SAT}} + V_{\mathrm{margin}}$ due to the use of cascode; or V_T, due to the use of common-source amplifier; or both. In addition, the use of positive feedback can result in instability and is generally awkward to implement in a fully differential topology.

The three techniques previously described improve gain by increasing the output resistance and therefore are unsuitable for driving resistive loads. The use of source follower as the output buffer compromises the output swing further and hence is not an attractive option for driving resistive loads. Moreover, the increased output resistance makes the amplifier susceptible to stray conductance effects, such as impact ionization and leakage currents.

Switched-capacitor techniques [8], [9] can be used to reduce the finite-gain error. However, they are useful only in limited applications. Furthermore, the switched-capacitor techniques require an additional clock cycle to remove the finite-gain error, and the improvement is strongly affected by input capacitance of the op amp [8] or by the common-mode rejection [9].

In this paper, we describe an effective open-loop gain-enhancement technique that does not require the use of cascode, thereby maximizing the output swing and the input common-mode range; and it does not require the use of long-channel transistors or subthreshold operations, thereby maximizing the speed. However, if desired, the technique can be used in combination with conventional techniques such as cascoding to further increase the open-loop gain. In addition, the gain enhancement remains effective even with moderate resistive loads. The gain-enhancement technique to be described can be used with any operational amplifier topologies, including two-stage, folded-cascode, and class AB—single ended or differential. In the following sections, we present the general gain-enhancement technique, followed by a two-stage implementation example chosen to demonstrate the technique in a low-voltage application. Although the technique is general and can be applied to most switched

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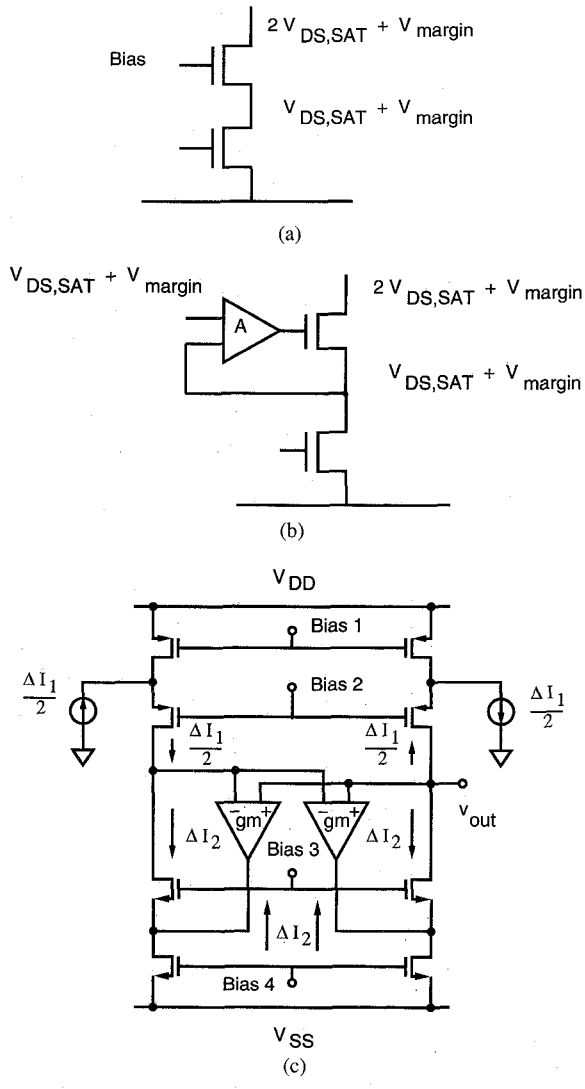

Fig. 1. Conventional gain-enhancement techniques. (a) A regular cascode circuit. (b) An active cascode circuit. (c) A positive feedback circuit.

capacitor circuits, our discussion will focus on continuous-time operation.

II. Principle of the Replica-amp Gain Enhancement

A. Transconductance Building Block

For the purpose of discussion, consider a transconductance amplifier with a finite output resistance r_o. As an example, an inverting amplifier using such a transconductance amplifier is shown in Fig. 2, with feedback.

Assuming that the elements Zf and Zg are capacitors and the initial charges on the capacitors are zero, the low-frequency output voltage is given by

$$v_O = -\beta\left(\frac{1}{1+\frac{1+\beta}{a_o}}\right)v_I \cong -\beta(1-\epsilon)v_I \tag{1}$$

where $\beta = \frac{Zf}{Zg}$, the ratio of the two impedances in the feedback network, and the low-frequency open-loop voltage gain $a_o = g_m r_o$. It can be seen from (1) that the finite gain

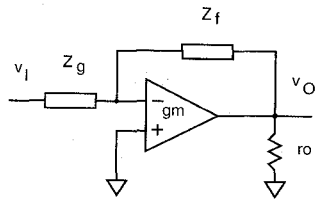

Fig. 2. An inverting op amp.

a_o produces an error ϵ given by

$$\epsilon = \frac{1+\beta}{a_o}. \tag{2}$$

(2) states that the error decreases as the open-loop gain increases. In the limit when the open-loop gain goes to infinity, the finite-gain error goes to zero, and the output achieves an ideal voltage of $-\beta v_I$.

B. Basic Description of the Gain-Enhancement Technique

Fig. 3 shows the enhancement technique using a replica amplifier RA. For simplicity, we first assume that Δr_o is zero, in which case the replica amp is identical to the main amplifier MA and has the same feedback network as MA. The input voltage v_I is applied to both MA and RA in parallel. Since RA is used in the same inverting configuration as the simple op amp shown in Fig. 2, the output voltage of the replica amplifier v_{Or} is already very close to the ideal output voltage within the finite-gain error given in (2). Since the coupling transconductance amplifier CA is connected in parallel with the inputs of the replica amplifier, CA produces a current i_X, which is the same as the current i_X produced by RA. This current i_X from CA is injected into the output resistance r_o of the main amplifier, producing a voltage that is already close to the ideal voltage. Therefore, MA provides only a small amount of error current Δi_X to bring the output voltage even closer to the ideal voltage of $-\beta v_I$. Since the input voltage needs to change by only a small amount to produce Δi_X, the effective open-loop gain is increased. Analysis shows that the dc output voltage of the main amplifier is

$$v_{Om} \cong -\beta\left(\frac{1}{1+\left(\frac{1+\beta}{a_o}\right)^2}\right)v_I \tag{3}$$

corresponding to an error given by

$$\epsilon \cong \left(\frac{1+\beta}{a_o}\right)^2. \tag{4}$$

Comparing (2) to (4), we see that the error term has been reduced by the factor of $\frac{a_o}{1+\beta}$, increasing the effective open-loop gain by the same factor. When the closed-loop gain β is small and a_o is large, the enhancement factor is potentially very large. In such cases, the actual improvement is limited by the matching between the main and the replica amps, as will be shown later.

C. Minimizing Power and Chip Area

The coupling amplifier CA, though shown as identical to both MA and RA, can be implemented with just a single

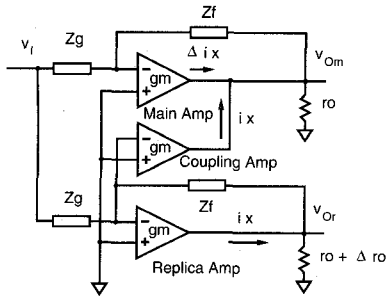

Fig. 3. A replica-amp gain-enhancement technique.

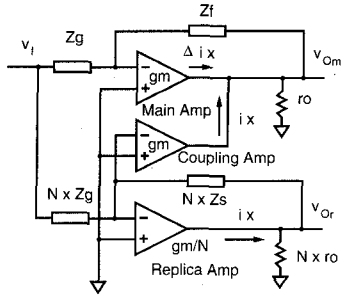

Fig. 4. Minimizing power and area by scaling down the replica amplifier.

transistor, as will be demonstrated in the two-stage example. In addition, RA need not be identical to MA. In Fig. 4, the transistors of the replica amplifier are scaled down by a factor of N in width from those of the main amplifier. The feedback network is also scaled by the same factor. As a result, the additional amount of chip area and power due to the addition of the replica amplifier can be minimized. Analysis shows that the output voltage in this case is unchanged from that given in (3). It is estimated that the replica amp can be scaled down in width by a factor of about 3 without significantly increasing the input-referred noise of the amplifier.

D. Effect of Mismatch

Previous analyses for Figs. 3 and 4 assume that MA and RA are perfectly matched. In practice, mismatch limits the gain-enhancement factor. Since mismatch is most likely dominated by the mismatch in output resistance, we consider this effect when the output resistance of RA in Fig. 3 is $r_o + \Delta r_o$, where Δr_o is no longer zero. It can be shown that

$$v_{Om} \cong -\beta \left(\frac{1}{1 + \left(\frac{\Delta r_o}{r_o}\right)\left(\frac{1+\beta}{a_o}\right)} \right) v_I, \text{ assuming } \frac{r_o}{\Delta r_o} \ll \frac{a_o}{1+\beta}. \tag{5}$$

Comparing (1) with (5), we see that the error due to finite gain is reduced by

$$\text{gain enhancement factor} = \frac{r_o}{\Delta r_o} = \frac{1}{\Delta}. \tag{6}$$

As can be seen from (6), for a 5% mismatch between MA and RA, the effective gain-enhancement factor is 20. Other sources of mismatch can be similarly analyzed.

E. Gain Enhancement when Resistively Loaded

Conventional gain-boosting techniques such as cascoding increase the gain by increasing the output resistance. Amplifiers built with such techniques suffer significant gain reduction when they drive resistive loads. In contrast, Fig. 5 shows the case when the present technique is used with two identical external resistive loads R_L added to both MA and RA. Analysis shows that even when R_L is many times smaller than r_o, the effective open-loop gain of MA remains almost unchanged. When R_L is more than an order of magnitude smaller than r_o, the effective open-loop gain does go down, though the gain enhancement remains effective. The enhancement factor in this case is $\frac{g_m R_L}{(1+\beta)}$. This analysis is predicated on the fact that the resistive loads are matched much better than the output resistance of MA and RA. This condition is generally satisfied, since typical on-chip poly resistors are much better matched than the output resistance of MOS transistors; and for off-chip resistive loads, the resistors can also be closely matched.

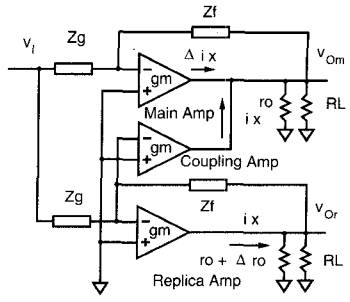

Fig. 5. A moderate resistive load does not degrade effective open-loop gain.

III. Circuit Implementation

A. Circuit Description

The technique described above can be applied in principle to any operational amplifier built with transconductance stages. To demonstrate the concept, a two-stage op-amp topology without cascode is chosen to maximize the output swing. In Fig. 6, the top half of the circuit is the main amp and the bottom half is the replica amp. For simplicity, no scaling is used, and RA is an exact replica of MA if we ignore the small dashed box near the output of RA. We will return to that box later. The external feedback networks are such that the same ratio β is maintained between MA and RA. Although a single-ended topology is chosen, the application of the replica-amp gain enhancement technique to a fully differential topology is straightforward. All the transistors used are of minimum gate length of 1.2 μm, with the exception of the output PMOS current source transistors MP4 and MPX4, which have a gate length of 1.8 μm. In a two-stage op-amp design, though the gain-boosting technique can be applied to the first, the second, or both stages, for simplicity the technique is applied only to the second stage.

The coupling amplifier is implemented with just a single transistor, MN4, which is connected in parallel with the second stage of RA. Since MN4 and MNX3 are connected in parallel, with 0 V applied to the input of the main amp, MN4 already provides the necessary current such that the output of the main amp is the same as that of the replica amp. This output voltage differs from the ideal value by the small error voltage given by (2). Therefore, transistor MN3 provides a small amount of error current Δi_X. As a result, for a given output voltage,

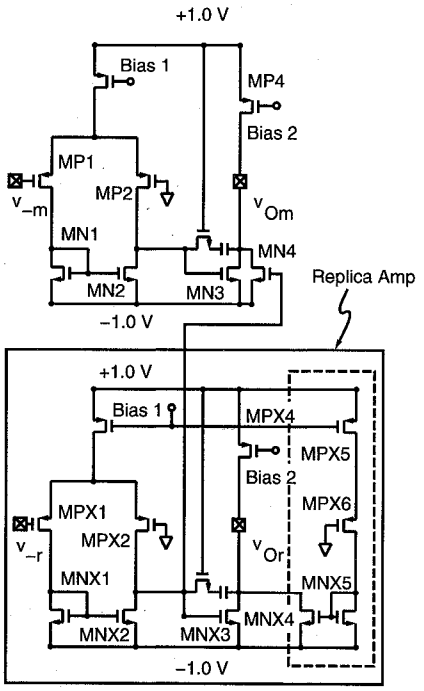

Fig. 6. Schematic of the op amp.

TABLE I
EXPERIMENTAL PERFORMANCE SUMMARY OF THE TWO–STAGE OP AMP

	Main Amp	Replica Amp
Channel Length:		
MP1, 2	1.2 μm	1.0 μm
MP3, 4	1.2 μm	1.1 μm
Feedback Network:		
C_f	10.0 pF	10.0 pF
C_g	10.0 pF	10.1 pF
C_c	10.0 pf	9.9 pF

TABLE II
SOURCES OF MISMATCHES USED IN SPICE SIMULATION

Enhancement	OFF	ON
Supply Voltage	±1 V	±1 V
Output Swing	100 mV from either rail	100 mV from either rail
DC Gain: no load	810	10 800
1 kΩ load	200	10 500
Power Dissipation	4 mW	9 mW
Settling Time (1% [gain-of-3 circuit]	55 ns	55 ns
Gain-Bandwidth	63 MHz	63 MHz
Load Capacitance	29 pF	29 pF
Die Area	0.34 mm^2	0.61 mm^2

only a very small amount of error voltage is necessary at the input of the main amp to drive the output of the main amp to the final level given by (3). Transistors MNX5, MPX5, and MPX6 in the small dashed box are added to mimic half of the input differential stage of the replica amp. Together, these transistors bias MNX4, resulting in MA and RA having the necessary matched output resistances.

B. Settling Time Considerations

Qualitatively, from Fig. 3, we see that MA and RA are driven in parallel by the input voltage v_I, each with its independent feedback network. In the worst case, we expect the settling time to be no more than the time it takes for the replica amp to settle first plus the time it takes for the main amp to settle. In other words, the worst-case settling time is 2 τ_s, where τ_s is the settling time when no enhancement is applied using a replica amp. Therefore, there is no possibility of any settling components slower than 2 τ_s. In practice, MA and RA settle more or less in parallel, so the actual settling time is less than 2 τ_s. A more rigorous quantitative analysis for a two-stage op amp is shown in Appendix I. The analysis indicates that in closed loop, the added poles are at the same location as the original poles without the replica-amp gain enhancement. It is shown that if the replica amp has the same load capacitance as the main amp, the settling time is approximately 1.3 τ_s. In the limit, when the replica amp load capacitance is reduced to zero, the settling time is essentially just 1 τ_s, the original settling time of the unenhanced op amp. Due to the difficulty of measuring settling accuracy at and greater than .1% at tens of MHz speed, SPICE simulation is used to demonstrate the validity of the analytical results summarized in Appendix I. In addition, although Appendix I assumes only a single mismatch in the output resistance, to account for multiple sources of mismatch in any physical implementation of the op amp the channel lengths of the transistors are mismatched, as shown in Table II, resulting in mismatches in g_m, device capacitance, and output resistance. In addition, 1% mismatches in both C_g and C_c are also introduced between the main and the replica amps. In order to separate the effect of final dc-gain error from the dynamic part of the settling, Fig. 7 shows the percentage difference between the output voltage as a function of time and the final output voltage. Due to the value of the nulling resistor used, one of the two poles shown in Appendix I for the unenhanced op amp is canceled, resulting in a first-order system. Since the Y-axis in Fig. 7 is on a log scale, first-order settling behavior will be a straight line with a slope inversely proportional to the time constant. Ignoring the slight ringing of the gain-enhanced op amp, Fig. 7 shows that both op amps have similar slopes, indicating that the time constant of the exponential decay are similar in both cases. For eight orders of magnitude in the percentage settling, the worst-case increase in settling time is about 16%. This SPICE result supports our qualitative reasoning as well as quantitative analysis of the replica-amp technique.

C. Noise Contribution from the Replica Amplifier

In Fig. 8(a), the noise contribution from RA is considered. $S_{n,\text{main}}$ is the spectral noise density at the input of MA, when RA is disconnected. $S_{n,\text{rep}}$ is the spectral noise density at the input of RA. H_{11} is defined as the voltage transfer function from the input of MA to the output of MA. H_{21} is defined as the voltage transfer function from the input of RA, through the coupling amp depicted as the dashed line, to the output of MA. The effective input-referred spectral noise density, $S_{n,i}$ is given by

$$S_{n,i} = S_{N,\text{main}}(j\omega) + \left|\frac{H_{21}(j\omega)}{H_{11}(j\omega)}\right|^2 S_{N,\text{rep}}(j\omega). \quad (7)$$

Fig. 8(b) shows the magnitude of H_{11} and H_{21} using SPICE.

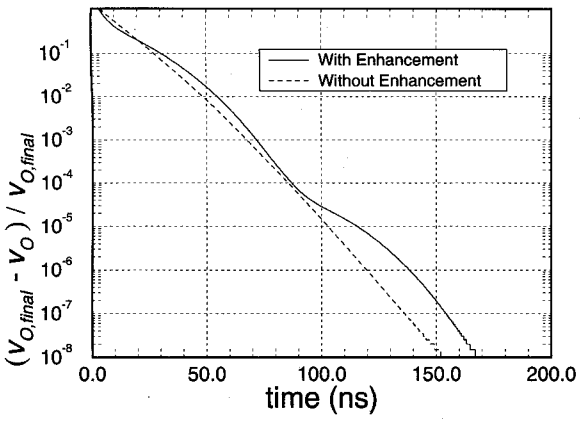

Fig. 7. SPICE simulation of the settling behavior.

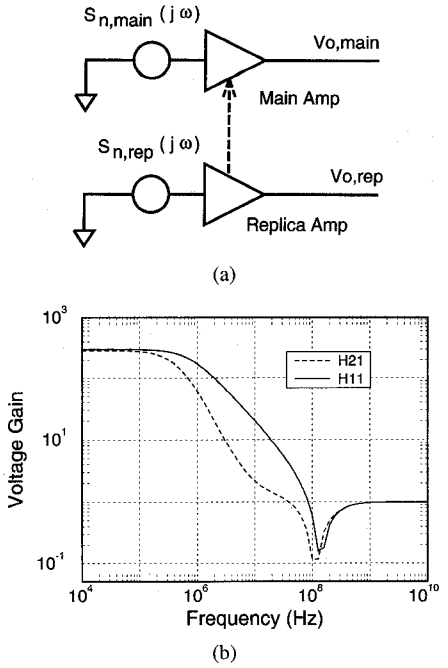

Fig. 8. Noise contribution from the replica amplifier. (a) Equivalent circuit for noise calculation. (b) Voltage transfer functions H_{11} and H_{21}.

For frequency range above 100 KHz, $|H_{21}| \ll |H_{11}|$. Hence, from (7), it can be seen that the noise contribution from the replica amplifier to $S_{n,i}$ is negligible. Although for low frequency, $1/f$ noise will be increased, in applications such as switched capacitor circuits the low-frequency noise can be removed using standard offset cancellation techniques.

IV. Experimental Results

The CMOS operational amplifier shown in Fig. 6 is fabricated in a standard 1.2-μm N-well digital CMOS process with single poly and double metal. The test circuit shown in Fig. 9 is used to characterize the performance of the op amp using $\pm$ 1-V supplies. For the main amplifier, an external effective capacitance of 22 pF in parallel with the effective capacitance from the feedback network gives a total load of 29 pF. The total load capacitance of the replica amp is approximately 19 pF. Fig. 10 shows the step response of the test circuit. The vertical resolution is 200 mV/div, while the horizontal resolution is 50 ns/div. The 1% settling time is measured to

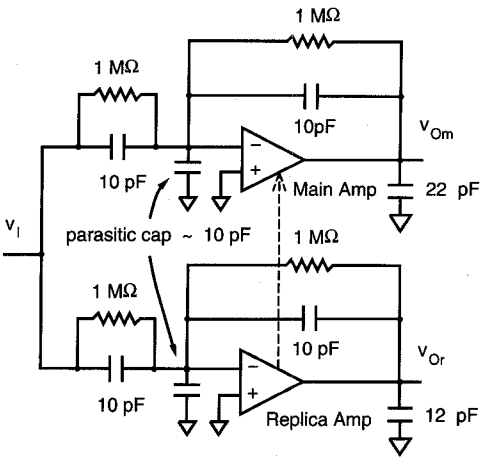

Fig. 9. Test circuit.

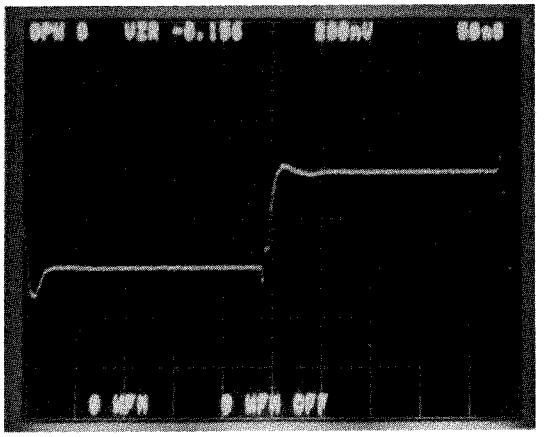

Fig. 10. Transient response.

be 55 ns. Within the resolution of the measurement setup, no significant difference in settling time is observed in the unenhanced amplifier with similar loading. This agrees with the theoretical analysis outlined in Appendix I as well as the simulated result.

Table II summarizes the measured performance at supplies of $\pm$ 1 V. As indicated, the output can swing within 100 mV from either supply rails. The effective dc gain is increased by a factor of approximately 13 with no load resistor. When a 1-kΩ resistor is added to both MA and RA, the gain drops from 810 to 200 for the unenhanced amplifier. However, when the enhancement circuit is turned on, the gain remains at greater than 10 000. It should be noted that the output resistance r_o of the amplifier is estimated to be 3 kΩ due to high current and short-channel transistors. Thus, the 1 kΩ load resistance represents approximately $\frac{r_o}{3}$. This result demonstrates the effectiveness of the replica-amp technique when resistive loads have to be driven. The power and the die area are approximately twice those without enhancement. However, as we have shown, scaling of the replica amplifier can be used to reduce both the power and the area consumptions.

Fig. 11 shows the die photograph. The chip contains two versions of the same amplifier. The version at the bottom part of the chip is scaled down by a factor of 10 for use with smaller capacitors. The experimental results were obtained from the bigger amplifier shown at the top of the chip. MA and RA are at the top and bottom half of the active area. As can be

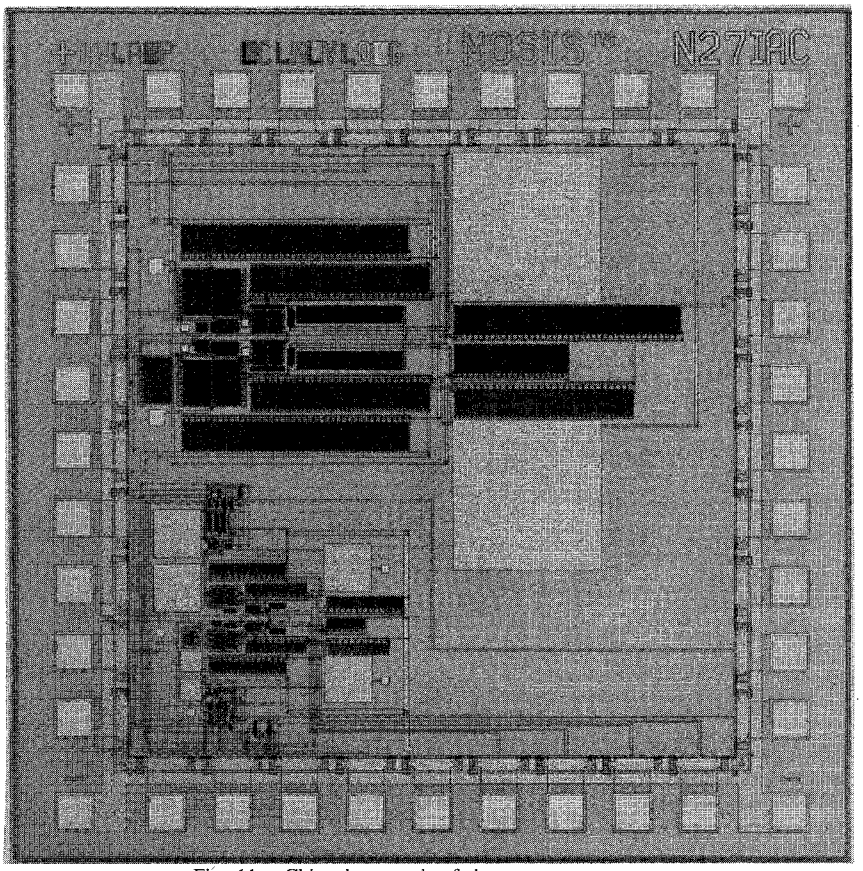

Fig. 11. Chip photograph of the two-stage op amp.

seen, since no scaling is used for simplicity, MA and RA are identical. Due to the lack of a second-layer poly, the 10-pF metal-poly compensation capacitors occupy a large area.

V. Conclusion

Conventional gain-enhancement techniques such as cascoding increase gain at the expense of reduced swing, which can be a major sacrifice in low-supply applications. In addition, since the gain is increased by increasing the output resistance, they are sensitive to impact ionization and resistive loads. In contrast, we have described a technique that increases the gain by matching the main and the replica amplifiers. This technique is general and can be applied to any op amp using transconductance stages. A two-stage topology was chosen to demonstrate the technique in a high-swing, low-supply application. We have shown experimentally that the op amp can be operated at $\pm$ 1-V supplies, with a dc gain of greater than 10 000, with or without 1-kΩ resistive loads. Qualitative and quantitative analyses indicate that the technique has only a small effect on the settling time, especially if the capacitive load of the replica amp is small compared to that of the main amp. In view of the current trend of ever decreasing supply voltages, the technique offers an attractive alternative to the conventional gain-enhancement methods.

Appendix I

The settling time of an operational amplifier typically consists of the initial slew-rate component and the final small-signal component. In order to show that the replica amplifier has only a small effect on the settling time of the main amplifier, we first note that the gain-enhancement technique does not effect the slew-rate behavior appreciably. Consequently, we focus on the effect of the replica amp on the small-signal component of the settling time. A simplified small-signal model shown in Fig. 12 is used for a two-stage op amp. The top half is the main amp, while the bottom half is the replica amp. The coupling amp, which is connected in parallel with the second stage of RA, is modeled as a voltage-controlled current source with a transconductance of g_{m2c}. R_{Lm} and R_{Lr} represent the parallel connection of the output resistance of the amplifier and any load resistor for the main and replica amplifiers, respectively. The buffers labeled X1 in series with the pole-splitting compensation capacitors C_{cm} and C_{cr} are added to simplify the analysis by eliminating the right-half-plane zeros typically encountered in two-stage op amps. In the actual implementation of the circuit, the right-half-plane zeros are removed by the nulling resistors as shown in Fig. 6. Assuming the loading of the capacitive feedback network is negligible, the replica amp has an open-loop transfer function given by

$$\frac{v_{or}}{v_{-r}} = -\frac{a_r}{\tau_{1r}\tau_{Lr}s^2 + \tau_R s + 1} \tag{8}$$

where

$$\begin{aligned} a_r &= g_{m1r}g_{m2r}R_{1r}R_{Lr}, \\ \tau_{1r} &= R_{1r}(C_{1r} + C_{cr}) \cong R_{1r}C_{cr}, \\ \tau_{Lr} &= R_{Lr}C_{Lr}, \text{ and} \\ \tau_R &= \tau_{1r} + \tau_{Lr} + g_{m2r}R_{Lr}R_{1r}C_{cr}, \\ &\cong g_{m2r}R_{Lr}R_{1r}C_{cr}. \end{aligned} \tag{9}$$

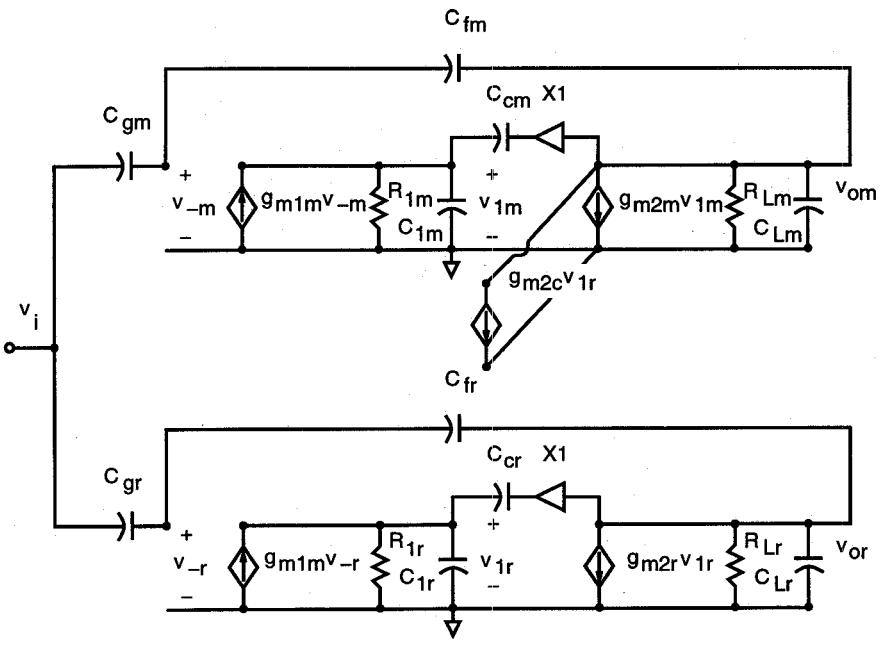

Fig. 12. Small signal model of a two-stage op amp.

Equation (8) shows a second-order system with the dominant pole at $-\frac{1}{\tau_R}$ and the nondominant pole at $-\frac{\tau_R}{\tau_{1r}\tau_{Lr}}$.

To investigate the effect of the replica amplifier on settling time, we first consider the closed-loop transfer function for the unenhanced case. We start with Black's formula, given by

$$A_{cl} = \frac{v_{om}}{v_i} = -f_2\left(\frac{a(s)}{1+a(s)f_1}\right) \tag{10}$$

where $a(s)$ is the open-loop transfer function similar to the negative of that defined in (8) and

$$f_1 = \frac{C_f}{C_g + C_f}, \text{ and}$$
$$f_2 = \frac{C_g}{C_g + C_f}. \tag{11}$$

It follows that the unenhanced closed-loop transfer function is given by

$$A_{cl,\text{unenh}} = \frac{v_{om}}{v_i} \cong -\frac{f_2 a_m}{\tau_1\tau_{Lm}s^2 + \tau_M s + f_1 a_m}. \tag{12}$$

The closed-loop poles are given by

$$s_{p,\text{closed}} \cong -\frac{g_{m2}}{2C_L} \pm j\frac{\sqrt{4f_1 g_{m1} g_{m2} C_c C_L - g_{m2}^2 C_c^2}}{2C_c C_L}. \tag{13}$$

We now consider the gain-enhanced case. Careful analysis [10] shows that when everything is matched except $R_{Lr} = R_{Lm}(1+\Delta)$, the effective open-loop transfer function for the main amp is given by

$$\begin{aligned} a_{m,\text{eff}} &= \frac{v_{om}}{v_{-m}} \\ &\cong -a_m(2\tau_1\tau_{Lm}s^2 + \tau_M s + f_1 a_m)/(\tau_1^2\tau_{Lm}^2 s^4 + 2\tau_1\tau_{Lm}\tau_M s^3 \\ &\quad + \tau_M^2 s^2 + f_1 a_m \tau_M s + \frac{1+f_1 a_m \Delta}{1+\Delta}). \end{aligned} \tag{14}$$

where we have used the fact that

$$\begin{aligned} f_1 &= f_{1m} = f_{1r}, \\ f_2 &= f_{2m} = f_{2r}, \\ \tau_1 &= \tau_{1m} = \tau_{1r}, \\ \tau_{Lm} &\cong \tau_{Lr}(1-\Delta), \\ a_m &= a_c = g_{m1r} g_{m2c} R_{1r} R_{Lm}, \\ a_m &\cong a_r(1-\Delta), \text{and} \\ \tau_M &\cong \tau_R(1-\Delta). \end{aligned} \tag{15}$$

From (14), the dc gain is given as

$$a_o \cong \frac{a_m}{\Delta} \tag{16}$$

which is consistent with (5) where $\frac{1}{\Delta}$ is the gain-enhancement factor.

The zeros are located at

$$s_z \cong -\frac{g_{m2}}{4C_L} \pm j\frac{\sqrt{8f_1 g_{m1} g_{m2} C_c C_L - g_{m2}^2 C_c^2}}{2C_c C_L} \tag{17}$$

where the subscripts m and r have been omitted from model parameters such as g_{m1} and C_L since the main and the replica amps are assumed to match.

The dominant pole location can be shown to be at

$$s_{p,\text{dominant}} \cong -\frac{\Delta}{\tau_M} \tag{18}$$

which is lower than that of the unenhanced case by the gain-enhancement factor.

Again we derive the closed-loop transfer function for the replica-amp gain enhanced case by substituting (14) into Black's Formula:

$$A_{cl,\text{enh}} = \frac{v_{om}}{v_i} \cong -\frac{f_2 a_m(2\tau_1\tau_{Lm}s^2 + \tau_M s + f_1 a_m)}{(\tau_1\tau_{Lm}s^2 + \tau_M s + f_1 a_m)^2} \tag{19}$$

Comparing (12) to (19), it can be seen that instead of one pair of complex poles given by (13), we have two coincident pairs. In addition, there is a pair of closed-loop complex zeros given by (17). For the purpose of discussion, we have assumed the poles and zeros given respectively by (13) and (17) are complex. The case when they are real can be similarly considered.

The closed-loop zero and pole locations characterize the settling behavior when the op amp is used in a feedback configuration. For a complex-pole pair $-\alpha \pm j\omega$, the dynamic component of the step response takes the form of $e^{-\alpha t}\cos(\omega t + \theta)$, where $\theta = \tan^{-1}\frac{\omega}{\alpha}$. Since the imaginary part of the pole location governs the ringing frequency, while the real part governs the decay of the exponential envelope, for simplicity, we consider only the real part in settling time considerations. (13) and (17) show that the real part of the zeros is at half the frequency of the poles. It can be shown that the decay of the exponential envelope to 0.1% is about 30% longer in (19) than in (12). This confirms our intuition that the replica amp cannot slow down the main amp by more than a factor of two.

For simplicity, we have ignored the loading effect of the feedback capacitors in the previous analysis. However, detailed analyses show that the feedback capacitors have no significant effect other than increasing the effective load capacitance by $\frac{C_g C_f}{C_g + C_f}$.

The above analysis assumes that the replica amp has the same capacitive load as the main amp. By reducing the capacitive load of the replica amp, the settling time can be further improved. A similar analysis can be carried out with $C_{Lr} < C_{Lm}$. In the limit when C_{Lr} is zero, we get the closed-loop voltage transfer function:

$$A_{cl,\text{enh}} = \frac{v_{om}}{v_i} \cong -\frac{f_2}{f_1}\left(\frac{\tau_M s + f_1 a_m}{\frac{\tau_M}{f_1 a_m}s + 1}\right)\left(\frac{1}{\tau_1 \tau_{Lm} s^2 + \tau_M s + f_1 a_m}\right) \tag{20}$$

Hence, it can be seen that the real pole-zero pair cancels, leaving a pair of complex poles at the original locations given by (13), when no replica amp is used. Since the pole-zero pair frequency is comparable to the closed-loop bandwidth, even if there is a slight mismatch there is no appreciable settling time increase. Therefore, by decreasing the replica amp load capacitance, the settling time can be made to be much less than a 30% increase predicted by the previous analysis. In our implementation, the replica amp capacitive load is significantly lower than that of the main amp. Hence, the gain enhancement has only a small effect on the settling time.

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