A 15-b 1-Msample/s Digitally Self-Calibrated Pipeline ADC

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***Abstract*—A 15-b 1-Msample/s digitally self-calibrated pipeline analog-to-digital converter (ADC) is presented. A radix 1.93, 1 b per stage design is employed. The digital self-calibration accounts for capacitor mismatch, comparator offset, charge injection, finite op-amp gain, and capacitor nonlinearity contributing to DNL. A THD of −90 dB was measured with a 9.8756-kHz sine-wave input. The DNL was measured to be within ±0.25 LSB at 15 b, and the INL was measured to be within ±1.25 LSB at 15 b. The die area is 9.3 mm × 8.3 mm and operates on ±4-V power supply with 1.8-W power dissipation. The ADC is fabricated in an 11-V, 4-GHz, 2.4-μm BiCMOS process.**

I. Introduction

PIPELINE analog-to-digital converters (ADC's) present advantages compared to flash or successive approximation techniques because potentially high resolution and high speed can be achieved at the same time. A 1-b-per-stage design is particularly amenable because each stage is very simple and fast. The primary limitations on the accuracy of a switched-capacitor pipeline ADC are capacitor mismatch, charge injection, finite operational amplifier gain and comparator offset. Previous 1-b-per-stage ADC's, including algorithmic and pipeline ADC's, removed some of these errors by using extra clock cycles with ratio independent [1], reference refreshing [2], error averaging [3] and analog calibration [4] techniques. Although the analog calibration does not require extra clock cycles during normal conversions, a weighted capacitor array is needed for each stage to be calibrated. For pipeline ADC's, where many stages are calibrated, the added complexity and capacitive load is significant.

This paper presents a digital self-calibration technique based on a radix 1.93 and one comparator per stage conversion algorithm. A nonradix two conversion algorithm was previously employed in a successive approximation converter [5]. That technique required a precise external calibration source and hence could be factory calibrated only. The technique described here is self-calibrating, simple, and tolerant of comparator errors. The digital calibration presented here may be applied to pipeline or cyclic ADC architectures. A 1-b-per-stage or multi-b-per-stage design may be employed with either ADC architecture.

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The key advantage of the digital calibration reported in this paper is that the errors at the carry transitions are *directly* measured under the same condition as during the normal conversion. Therefore, this technique offers potentially higher calibration accuracy than other calibration techniques [6]–[8] that measure the error at different conditions than the actual conversion. Another important aspect of this design is that the calibration is performed in the digital domain, so no extra analog circuitry, such as weighted capacitor arrays, is needed and no extra clock cycles are necessary during the conversion [9], [6]. The digital calibration reported here automatically accounts for capacitor mismatch, capacitor nonlinearity contributing to DNL, charge injection, finite op-amp gain, and comparator offsets. The nominal offsets of the op amp and comparator are reduced by standard offset cancellation and subsequently eliminated by digital calibration.

Unlike analog calibration, digital calibration does not correct or create analog decision levels. Therefore, the uncalibrated ADC must provide decision levels spaced at no more than 1 LSB at the intended resolution. In 1-b-per-stage pipeline ADC's, missing decision levels result when the input of any of the stages exceeds the full scale due to capacitor mismatches, capacitor nonlinearity, charge injection, finite op-amp gain and comparator offsets. The missing decision levels cannot be removed by digital calibration alone. Missing decision levels can be eliminated, however, by using gain less than 2 and two to three more stages of pipeline, which gives enough redundancy in the analog decision levels. With gain less than 2, missing codes are introduced rather than missing decision levels. The missing codes that result with a gain less than 2 are eliminated by the digital calibration. In contrast to an elaborate calibration reported previously using gain less than 2 [9], the calibration reported here is much simpler and more accurate. No multiplication is needed in the calibration algorithm, and only a small digital memory is needed.

II. Pipeline Architecture

The pipeline architecture used is shown in Fig. 1. A 1-b-per-stage design is employed. The pipeline begins with a sample-hold amplifier (SHA) and is then followed by multiply-by-two (MX2) stages. The prototype ADC consists of an input SHA and 17 MX2 stages that provide decision level redundancy for a 15-b resolution. Each MX2 stage has an analog input and a 1-b digital input as well as an analog output and a 1-b digital output. The gain-of-1 and gain-of-2 sampled-data functions for the SHA and the MX2 stages are, respectively, performed using operational amplifiers in switched-capacitor

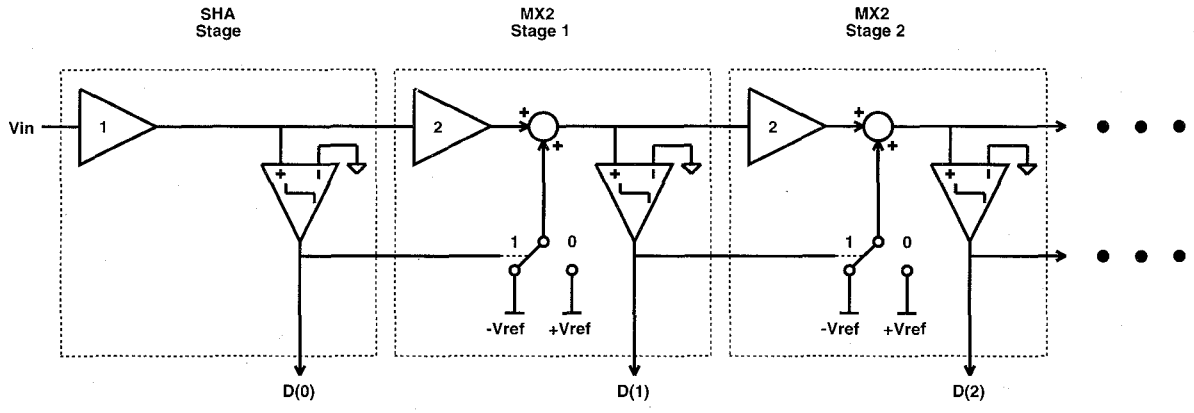

Fig. 1. Pipeline ADC architecture.

closed-loop configurations. The SHA and MX2 stages each utilize a comparator to determine the respective output bits. Only single-ended systems are drawn for simplicity, though the actual system is fully differential.

The radix 2 1-b-per-stage ADC algorithm is next explained. As shown in Fig. 1, the analog input V_{in} of the ADC is first sampled by the SHA. A comparator monitors the SHA output $V_{\text{out}}(0)$, resulting in $D(0) = 1$ if V_{in} is positive or $D(0) = 0$ if V_{in} is negative. The SHA output $V_{\text{out}}(0)$ is then passed to MX2 stage 1. Thus the input to MX2 stage 1 is $V_{\text{in}}(1) = V_{\text{out}}(0)$. The output $V_{\text{out}}(1)$ of MX2 stage 1 is $2V_{\text{in}}(1) - V_{\text{ref}}$ if $D(0) = 1$ or is $2V_{\text{in}}(1) + V_{\text{ref}}$ if $D(0) = 0$. A comparator monitors $V_{\text{out}}(1)$ in MX2 stage 1 and results in $D(1) = 1$ if $V_{\text{out}}(1)$ is positive; it results in $D(1) = 0$ if $V_{\text{out}}(1)$ is negative. These data are then passed on to the remaining MX2 stages in a similar manner. The description of some of the switched-capacitor circuits used to implement this basic radix 2 1-b-per-stage algorithm is found in [3].

III. Digital Self-Calibration Principle

A. Errors in Radix 2 Pipeline ADC

Fig. 2 shows the ideal residue and transfer characteristic for a radix 2 pipeline ADC. MX2 stage 11 is in focus and is assumed to be ideal. The remaining six stages of the pipeline are also assumed to be ideal. The residue plot shows the residue output V_{out} of a MX2 stage plotted as a function of the MX2 stage input V_{in} for the cases $D = 0$ and $D = 1$. The bit D is the bit $D(10)$ provided from MX2 stage 10. Note that the stage designation has been omitted from V_{in} and V_{out} for simplicity.

The word X is composed of bits $D(11)D(12)\cdots D(17)$ and is therefore the quantized representation of the residue output V_{out}. The output $D(10)D(11)\cdots D(17)$ is identified as the quantized representation of V_{in}. The digital output $D(10)D(11)\cdots D(17)$ is plotted as a function of V_{in}, resulting in an ideal transfer characteristic. Although $D(10)D(11)\cdots D(17)$ assumes discrete values, the transfer characteristic is plotted continuously for simplicity.

Fig. 3 shows the ideal residue plot and the effects of principal errors on the residue plot. The dashed box represents the reference boundary that passes through coordinates $\pm V_{\text{ref}}$

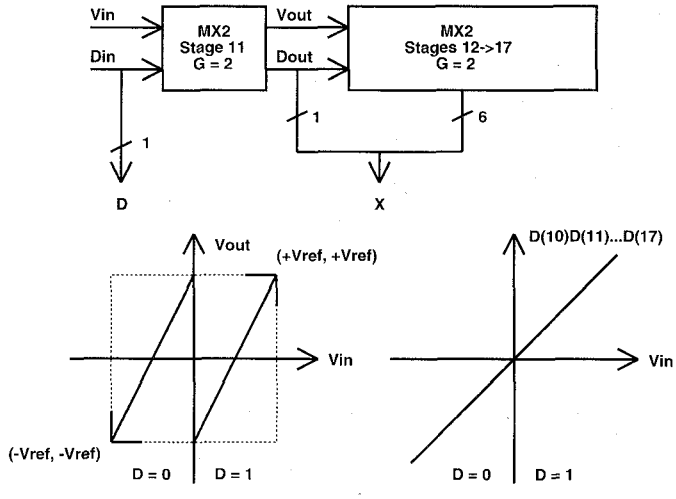

Fig. 2. Ideal residue and transfer characteristic of pipeline ADC.

along the V_{out} axis and $\pm V_{\text{ref}}$ along the V_{in} axis. Charge injection offset causes a vertical shift of the residue plot. Near the major carry transition point, the residue exceeds the reference boundary, resulting in missing decision levels. This is because the remaining pipeline section is saturated so that the output code does not change for the corresponding range of analog input. Near the major carry transition point, the residue minimum does not extend to $-V_{\text{ref}}$, resulting in a gap from the minimum to the reference boundary; missing codes result. This is because the full input range of the remaining pipeline section is not accessed. Comparator offset causes a shift of the major carry transition point. This leads to the residue exceeding the reference boundary as well as to a gap in the reference boundary. Again, missing decision levels and missing codes, respectively, result. Finally, capacitor mismatch as indicated causes the residue to exceed the reference boundary near the major carry transition point, resulting in missing decision levels. Capacitor mismatch could also lead to a gap from the residue extrema to the reference bou ndary near the major carry transition point, resulting in missing codes.

B. Motivation for Radix < 2 Pipeline

As discussed in the previous section, when the output of any stage in a radix 2 pipeline ADC exceeds $\pm V_{\text{ref}}$, missing

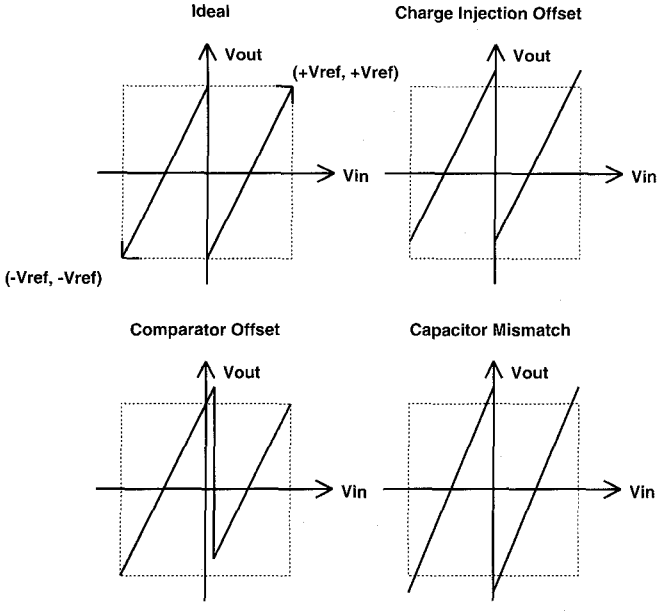

Fig. 3. Errors in radix 2 1-bit-per-stage ADC's. Missing codes and missing decision levels present.

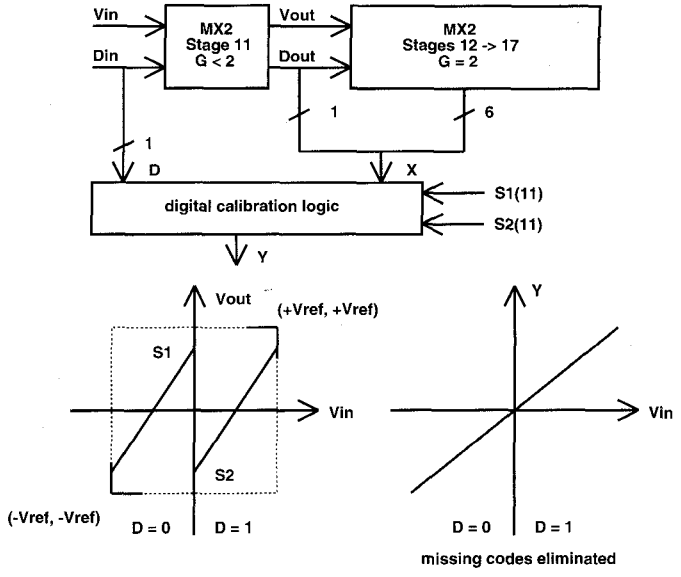

Fig. 4. Pipeline ADC with digital calibration applied to the eleventh stage.

decision levels occur, which cannot be eliminated by digital calibration alone. The key is to use a nominal gain of less than 2 such that the output of each stage never exceeds $\pm V_{\text{ref}}$. For the case of radix < 2, the principal errors affect the residue output in a similar manner as with radix 2. Since the residue is maintained within the reference boundary, no missing decision levels result. The missing codes that result due to the gaps from the residue extrema to the reference boundary are eliminated with digital calibration.

C. Digital Self-Calibration Algorithm

One of the primary objectives of the digital calibration is to eliminate ratiometric errors due to capacitor mismatch. The specific value of the reduced radix is not central to the operation of the digital calibration algorithm. In addition, the gains can be different among the stages to be calibrated. The gain must be reduced enough so that the residue is contained within the reference boundary. Excessive gain reduction decreases the total number of decision levels available and requires an excessive number of additional stages.

The pipeline ADC presented has the first 11 stages with nominal gains set to 1.93 and the last six stages with nominal gains set to 2. The calibration begins with the eleventh stage and continues with the tenth stage, up to the first stage. The gain of 1.93 was chosen to ensure enough gain reduction so that the residue never exceeds the reference boundary in the worst case when the maximum capacitor mismatch, comparator offset and charge injection error magnitudes are summed together.

Fig. 4 shows the pipeline ADC with digital calibration of the eleventh stage. The last six stages of the pipeline have nominal gains set to 2. In Fig. 4, the residue plot of MX2 stage 11 with gain reduction and zero comparator offset is shown. An exaggerated gain reduction is indicated for simplicity in illustration. The outputs D and X are presented to the digital calibration logic system along with calibration constants S_1 and S_2 determined for stage 11. The two quantities S_1 and S_2 are identified on the residue plot. S_1 and S_2 correspond to the quantized representation of V_{out}, or the quantity X, when $V_{\text{in}} = 0$ with $D = 0$ and $D = 1$, respectively.

The digital self-calibration algorithm is now described:

$$Y = X, \text{if } D = 0 \tag{1}$$

$$Y = X + S_1 - S_2, \text{if } D = 1 \tag{2}$$

where D is the bit decision, X is the raw code and Y is the transformed code. This transform ensures that the output code Y with $V_{\text{in}} = 0$ is the same for $D = 0$ and $D = 1$, eliminating missing codes. Note that no multiplication is required in this calibration scheme. Two constants S_1 and S_2 are needed per stage. The entire converter uses a 132-b memory to store $S_1 - S_2$ for each stage being calibrated. To determine S_1, the analog input is set to zero and the input bit is forced to 0. The quantity X in this condition is S_1. In an analogous manner, S_2 is determined when the input bit is forced to 1. The calibration constants S_1 and S_2 are each obtained by averaging 2 048 samples without truncation and then truncating the final result.

D. Digital Self-Calibration of Higher Level Stages

With the digital calibration of one MX2 stage accomplished, the digital calibration of higher level stages can proceed. Fig. 5 demonstrates the process. The system within the dashed box has been of principal interest thus far. The last six stages with nominal gain of 2 and the digital calibration logic were used to calibrate stage 11. The calibrated system within the dashed box is now used as an ADC to measure stage 10. Calibration constants S_1 and S_2 for stage 10 are determined in a similar manner as for stage 11. The digital calibration logic system for stage 10 follows the same algorithm as for stage 11. The calibrated system leading with stage 10 can then be used to calibrate stage 9. This process continues up

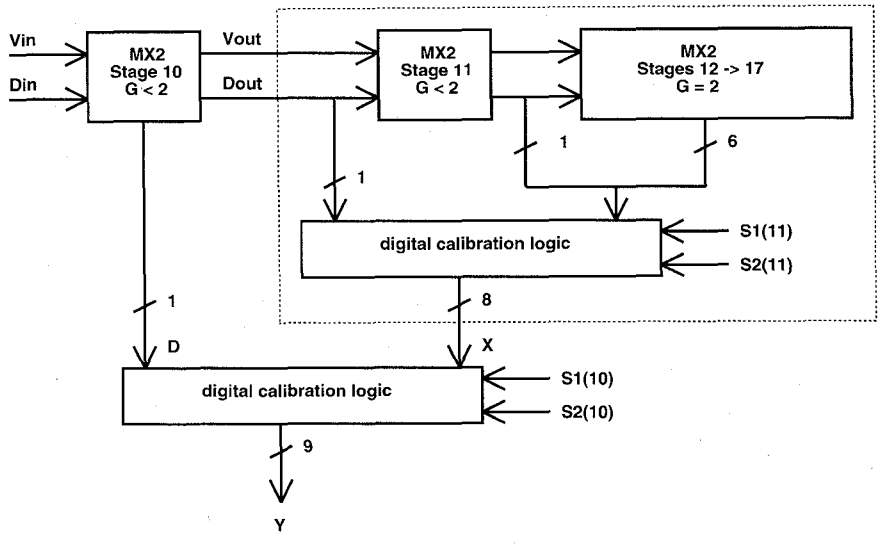

Fig. 5. Digital calibration of higher level stages.

to the first MX2 stage. In this way, the entire pipeline ADC is calibrated. Quantization and truncation errors are avoided by averaging the calibration data without truncation. The calibration algorithm described here results in an input referred offset. However, this offset is constant and hence eliminated by digitally subtracting the offset measured with 0 V at the SHA input.

Since the calibration *aligns* points S_1 and S_2 using measured values under the same condition as during normal conversion, the calibration automatically accounts for capacitor mismatch, charge injection and finite op-amp gain. Capacitor nonlinearity causes only integral nonlinearity (INL) error, not differential nonlinearity (DNL) error. It will be shown that comparator errors up to the gain reduction factor (3.5% of full scale) have no effect on the conversion accuracy. The nonunity gain that results from the radix < 2 pipeline can be easily compensated at the ADC digital calibration logic or elsewhere in the system. In the prototype ADC, input voltages corresponding to $\pm 0.95 V_{\text{ref}}$ give full-scale output codes for 15 b. Note that only digital addition, subtraction, and a small digital storage are needed for the digital calibration algorithm. With a 1 Msample/s conversion rate and 2 048-point averaging, the total calibration time for the converter is approximately 70 ms.

IV. Errors Corrected by Digital Self-Calibration

The principal property of the digital self-calibration technique is that it accounts for capacitor mismatch and charge injection, as explained in the previous sections.

Another important property of the digital calibration algorithm is that it is tolerant of comparator offset. Fig. 6 shows the residue plot for a radix < 2 MX2 stage with comparator offset present in the previous stage. As can be seen, the major carry transition point is shifted. The calibration constants S_1 and S_2 correspond to zero input. The calibration constants S_1' and S_2' correspond to the extrema of the residue plot near the major carry transition point. The key result is that $S_1' - S_1 = S_2' - S_2$. Thus, $S_1' - S_2' = S_1 - S_2$ so (2) remains

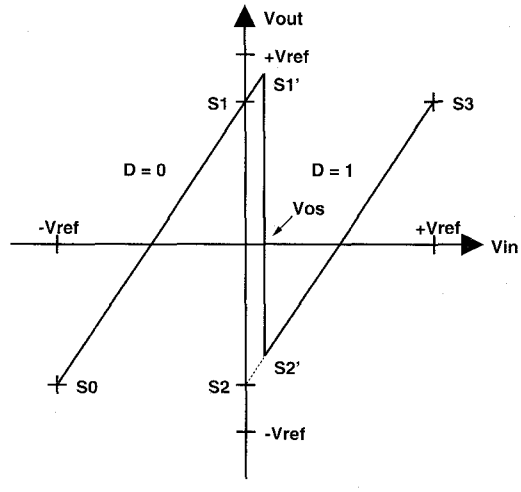

Fig. 6. Residue plot of a radix < 2 MX2 stage with comparator offset V_{OS} present in the previous stage.

unchanged. This is important because the comparator offset requirement can be relaxed. In the present design, comparator offset up to 1.75% of V_{ref} is corrected by calibration; this is equivalent to a 3.5% residue output referred error. Notice that the comparator offset in question can be static or dynamic. The digital self-calibration will remove this error as long as the comparator offset is low enough so that the residue does not exceed the reference boundary. It must be noted that when capacitor mismatch, charge injection and comparator offset are simultaneously present, the combined output referred error must remain less than 3.5% of V_{ref} for the calibration to be feasible.

A finite op-amp gain can be tolerated with the digital self-calibration. This effect represents a gain error and is not distinct from capacitor mismatch if the gain is finite, but constant. Temperature can cause the gain to drift and this will require recalibration. To avoid this need of recalibration, the pipeline ADC uses a high d-c gain op-amp design.

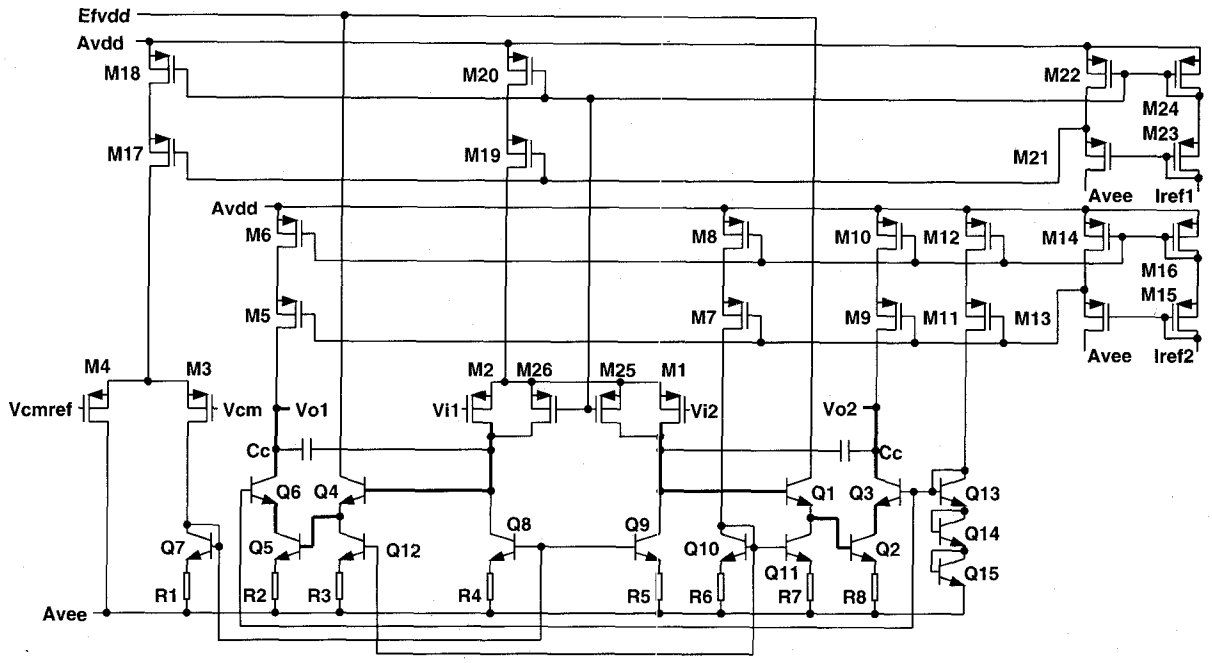

Fig. 7. Operational amplifier.

V. Circuit Design

A. Op Amp and Comparator Pre-Amp

BiCMOS is used to provide n–p–n bipolar devices for high-speed, high-gain analog capability while providing CMOS devices for a switched-capacitor environment. The operational amplifier is shown in Fig. 7. The op amp is a two-stage, fully differential design with a 100 MHz unity-gain bandwidth and a 125-dB dc gain [10]. The main signal path is indicated in bold. A PMOS differential input stage, composed of devices M_1 and M_2, is used for lower $1/f$ noise and lower threshold voltage relaxation, compared to NMOS [11]. Focus will be placed on the right half of the remainder of the op-amp signal path. An n–p–n bipolar second stage Q_2 is used to achieve a high-frequency nondominant pole. The second stage is cascoded with device Q_3 and then actively loaded with a cascoded current source, composed of devices M_9 and M_{10}, to obtain the high-output resistance used to help achieve large op-amp dc gain. This large dc gain is desirable to avoid the need for recalibration due to gain drift arising, for instance, from a temperature change. Device Q_1 is used as an emitter follower to prevent the second stage from excessively loading the first-stage output and thus reducing the dc gain. Compensation capacitor C_c is used for pole-split compensation of the op amp [12]. A dynamic common mode feedback scheme is used to sense the output common mode level of the op amp [10], [13]. The voltage $V_{\rm CM}$ represents the output common mode level. A differential pair composed of devices M_3 and M_4 is used to steer common mode current to the first stage of the op amp. This completes the common-mode negative feedback loop that tends to drive $V_{\rm CM}$ equal to $V_{\rm CMREF}$, thus stabilizing the output common-mode level. The voltage $V_{\rm CMREF}$ is set between the power-supply rails, or ground, for a positive and negative power-supply scheme. Devices M_{25} and M_{26} are used to avoid a start-up difficulty in the output common mode level when the power supply is turned on. If the output common mode level is near the $A_{\rm VDD}$ power-supply rail, then the input differential pair bias current source M_{19} could be cut off and the op-amp output common mode level could remain at the $A_{\rm VDD}$ power-supply rail. However, M_{25} and M_{26} turn on in this condition to drive the output common mode level away from $A_{\rm VDD}$, as desired. Once the output common mode level is stabilized, devices M_{25} and M_{26} remain cut off for normal op-amp operation.

The comparator preamplifier is shown in Fig. 8. A two-stage, open-loop design is used. The main signal path is emphasized in bold. A PMOS differential input pair, composed of devices M_1 and M_2, is used for reasons analogous to those for the op amp. Focus will be placed on the right half of the remainder of the pre-amp signal path. Emitter follower Q_2 is used as a buffer between the first-stage output and the second-stage input. A bipolar differential pair, composed of devices Q_3 and Q_4, is principally used to achieve the gain in the pre-amp. Emitter follower Q_6 is used to prevent loading of the second-stage output. Devices Q_{7-10} are used to establish sufficient common mode input level to bases of Q_1 and Q_2 so that $V_{\rm CB}$ for Q_{13} remains positive. The comparator uses two preamplifiers in cascade, connected using coupling capacitors, which then drive a simple CMOS cross-coupled latch. Open loop offset cancellation [14] is used to reduce the input referred offset of the preamplifiers well within the calibration range. The gain of each preamplifier is approximately 60. Since passive loads are used in the preamplifier design with low gain, a common mode feedback scheme is not required.

B. Pipeline ADC Timing

The basic pipeline ADC timing is shown in Fig. 9. Two-phase, nonoverlapping clocks ϕ_1 and ϕ_2 are used. The analog

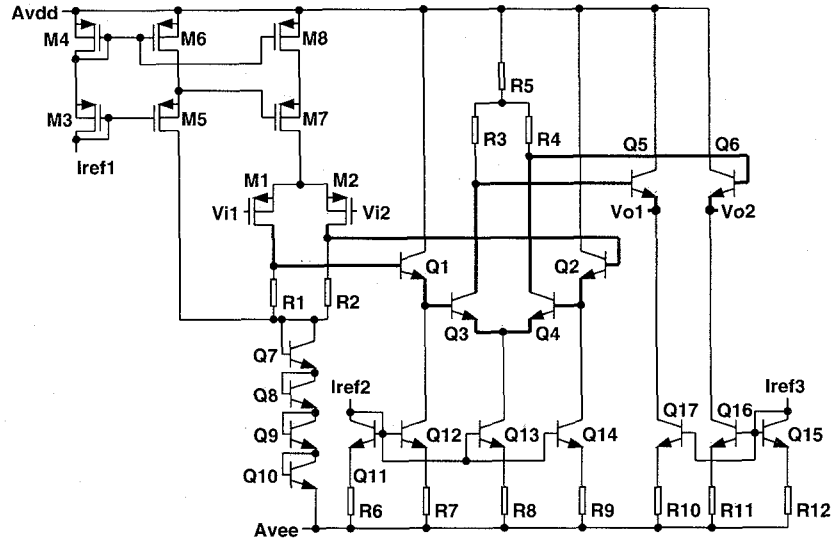

Fig. 8. Comparator pre-amplifier.

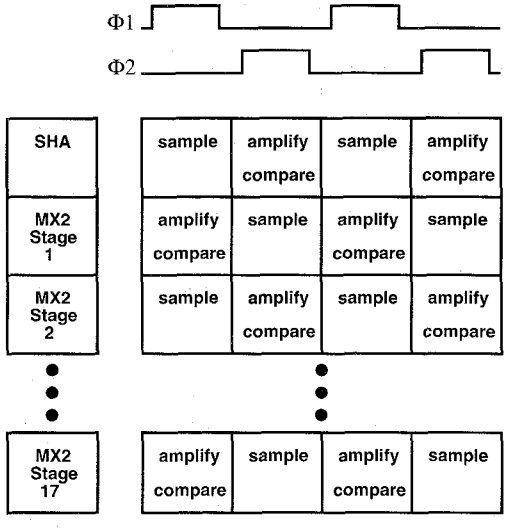

Fig. 9. Pipeline ADC timing.

input to the pipeline ADC is presented to the SHA while ϕ_1 is high. At the end of phase ϕ_1, the analog input is sampled. When ϕ_2 is high, the SHA switches to the amplify mode and its output is presented to the input of MX2 stage 1. At the end of phase ϕ_2, the analog input presented to MX2 stage 1 is sampled. Also at the end of phase ϕ_2, the comparator monitoring the output in the SHA is strobed and the input bit $D(0)$ for MX2 stage 1 is determined. This process continues until the ADC input data in question reaches the end of the pipeline. New ADC input data is sampled at the end of each phase ϕ_1. Thus, the throughput of the ADC is the period of the clock, or 1 μs. The latency of the ADC is 18 clock periods, or 18 μs. Shift registers can be used to time align the pipeline output data.

C. Switched-Capacitor Multiply by Two

Fig. 10 shows an MX2 amplifier for an even-numbered stage in the (a) sample phase and (b) amplify phase. Although the actual implementation is fully differential, a single-ended version is shown for simplicity. The capacitors C_1 and C_2 are nominally equal. A small capacitor C_3, added in the circuit to reduce the nominal gain to 1.93, C_2 can be expressed as $C_2 = (1+\alpha)C_1$, where α indicates the mismatch between C_1 and C_2, thus $|\alpha| \ll 1$. Nominally, $C_3 = \beta C_1$ where $\beta = 0.035$. The top plates of the double-poly capacitors C_1, C_2, and C_3 are connected to the op-amp input. The nominal value of C_1 and C_2 is 1 pF. During the sample phase, the op amp is in the unity-gain connection and the analog input V_{in} is presented to the bottom plates of the input capacitors C_1 and C_2. The bottom plate of C_3 is grounded. During the amplify phase, the op amp is in the inverting connection with the bottom plates of capacitors C_2 and C_3 connected to the op-amp output, and the bottom plate of C_1 is connected to $+V_{\text{ref}}$ if $D = 1$ or $-V_{\text{ref}}$ if $D = 0$. Additional clock phases derived from the two-phase nonoverlapping clocks are used in order to minimize the charge injection in the SHA and MX2 stages [3]. Performing a charge balance between sample and amplify phases, for the case $D = 1$ the output can be shown to be

$$V_{\text{out}} = \frac{(2+\alpha)V_{\text{in}} - V_{\text{ref}}}{1+\alpha+\beta} \approx 0.965(2V_{\text{in}} - V_{\text{ref}}) \qquad (3)$$

VI. Experimental Results

The prototype ADC uses external logic circuits and software to perform the addition, subtraction, and data storage for the digital self-calibration algorithm. In order to operate the ADC, calibration data is first obtained. The converter is then run at the maximum possible speed. Calibration mode data and run mode data are obtained at 1 Msample/s. The chip was designed for a maximum sampling rate of 8 Msample/s. However, the present experimental set-up is limited to 1 Msample/s. It is surmised that the 121-pin PGA package utilized is the primary source of circuit settling degradation.

The total harmonic distortion (THD) is computed from the ratio of the non-sine-wave input spectral power up to the Nyquist rate, or 500 kHz, to the sine-wave power. Fig. 11

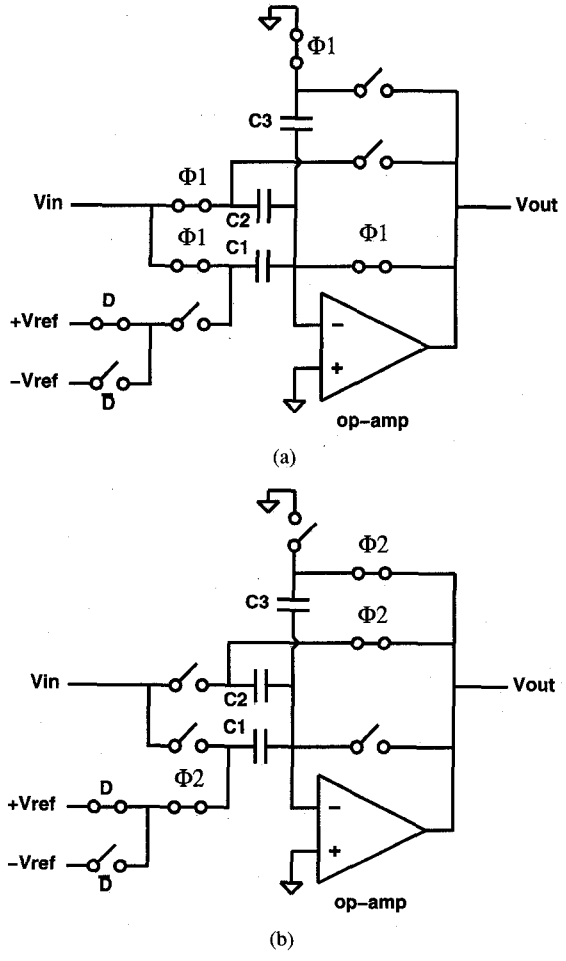

Fig. 10. Single-ended version of an MX2 amplifier for an even-numbered stage in the (a) sample phase and (b) amplify phase.

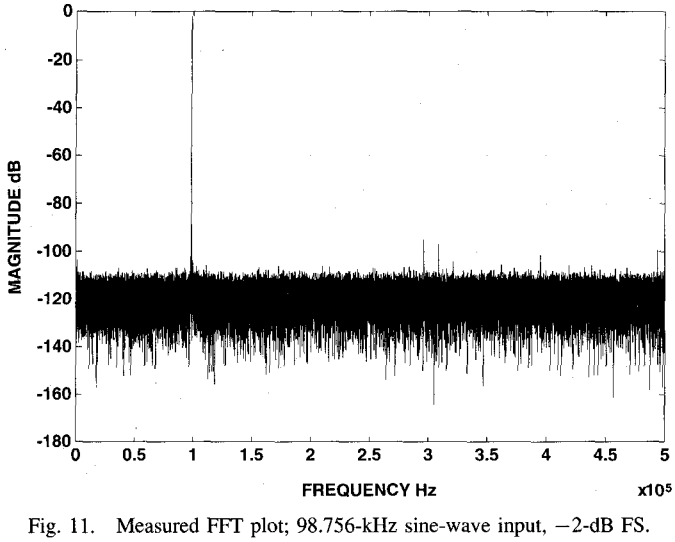

Fig. 11. Measured FFT plot; 98.756-kHz sine-wave input, −2-dB FS.

shows the FFT of the measured output data with a 98.756-kHz sine-wave input at −2-dB full-scale (FS) input. The THD in this case is −90 dB. The input frequency of 98.756 kHz is close to the limit of the sine-wave generator, which is rated at approximately −85 dB THD+N up to 100 kHz. The input referred noise of the ADC was measured as 1.25 LSB rms at

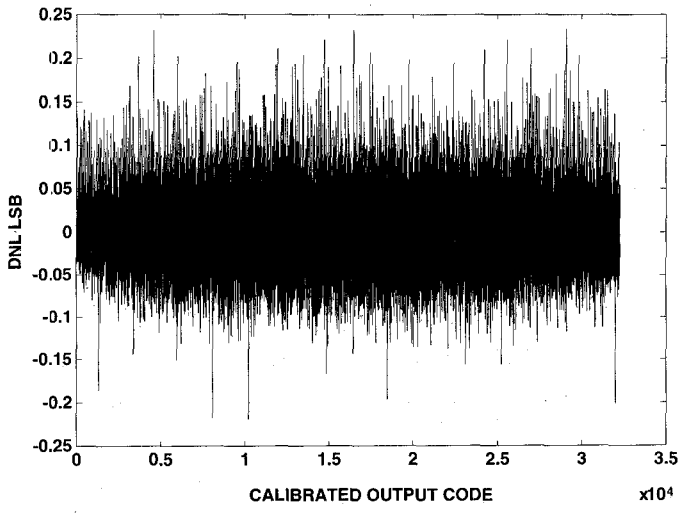

Fig. 12. Measured differential nonlinearity at 15 b.

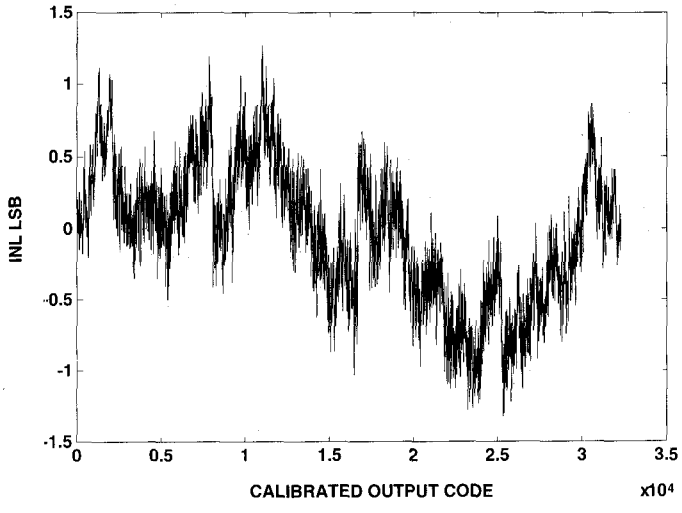

Fig. 13. Measured integral nonlinearity at 15 b.

15 b. Due to reduced power-supply operation and a capacitor voltage coefficient of 62 ppm/V, the differential reference voltage was limited to 4 V.

Fig. 12 shows the plot of the measured differential nonlinearity of the ADC. The peak DNL is within ±0.25 LSB. Fig. 13 shows the plot of the measured integral nonlinearity of the ADC. The peak INL is within ±1.25 LSB. The DNL and INL were obtained using a sine-wave code density test [15] with an FS sine-wave input at 9.8756 kHz. The sine-wave code density test was run for approximately 8 h collecting a 32 million sample histogram. Thus the INL shown in Fig. 13 reflects not only the capacitor voltage coefficient but also cumulative drift of the calibrated transfer characteristic over the 8-h period.

The power supply of ±5 V is reduced to ±4 V on some parts due to changes in the process ground rules. The power dissipation reflects two design parameters. First, the ADC operates on a ±4-V power supply. Second, to achieve high resolution, large capacitors are used, resulting in over 7 pF of loading for each operational amplifier. To settle to 15–16 b of accuracy at the target sampling rate of 8 MHz, relatively

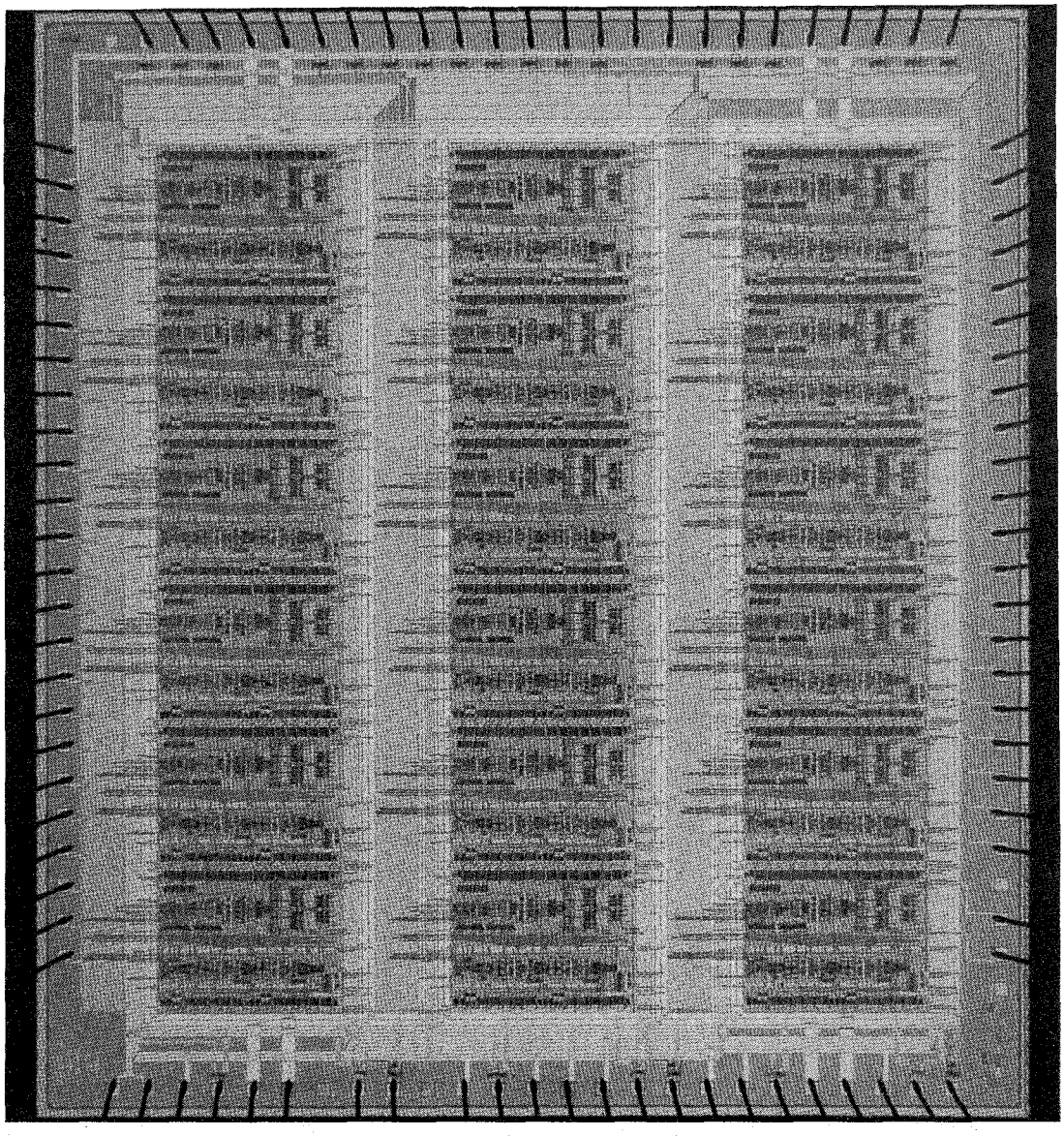

Fig. 14. Pipeline ADC die photo.

high power is necessary for the operational amplifier. Although capacitance and amplifier power can be scaled down for later stages of the pipeline, identical designs are employed for all 17 MX2 stages and the SHA for simplicity. No attempts were made to optimize the die area. Fig. 14 shows the die photograph of the ADC. The summary of performance parameters is listed in Table I.

TABLE I
CHIP PERFORMANCE

Resolution	15 b
Conversion Rate	1 Msample/s
THD	−90 dB
DNL	< ±0.25 LSB
INL	< ±1.25 LSB
Input Referred Noise	1.25 LSB rms
Input Range	4 V
Power Supply	±4 V
Power Dissipation	1.8 W
IC Dimensions	9.3 mm × 8.3 mm
Component Count	5 955
Process	11 V, 4 GHz, 2.4 μm BiCMOS

VII. CONCLUSION

This paper has demonstrated a digital self-calibration technique based on radix < 2 applied to a 1-b-per-stage pipeline ADC. This technique accounts for capacitor mismatch, comparator offset, finite op-amp gain, and for DNL error contributed by circuit nonlinearities. A 15-b, 1-Msample/s pipeline ADC prototype was demonstrated utilizing an 11-V, 4-GHz, 2.4-μm BiCMOS process. No component matching or offsets better than 7-b accuracy are needed to attain 15-b linearity with this technique. The digital self-calibration algorithm requires only addition, subtraction, and small data storage. This technique may be applied to pipeline or cyclic ADC architectures. A 1-b-per-stage or multi-b-per-stage design may be employed with either ADC architecture.

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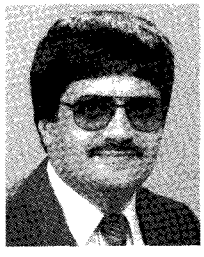

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