16-Channel Oversampled Analog-to-Digital Converter

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Abstract—**Oversampled Analog-to-Digital conversion has been demonstrated to be an effective technique for high resolution analog-to-digital (A/D) conversion that is tolerant to process imperfections. The area and power budget of conventionally designed oversampled analog-to-digital converters has precluded their application from areas where a large number of low frequency signals need to be converted simultaneously. A new oversampled A/D design methodology is proposed to cut the area and power budget per channel of an oversampled analog-to-digital converter. The design and implementation of a 16-channel oversampled analog-to-digital converter is presented which can be used as the core of the multichannel data acquisition system. The prototype achieved 80 dB of signal-to-noise-plus-distortion over 1 kHz, -80 dB of crosstalk and used less than 20 mW of power excluding clock generation.**

I. Introduction

In recent years, oversampled analog-to-digital converters have emerged as some of the most promising architectures for low-frequency high-resolution applications [1], [2]. This technique has been shown to reliably provide high resolution without trimming or high-precision components [3].

Oversampled converters consist of two main system blocks: the front end analog modulator and the digital decimator. The analog front end takes a bandlimited analog signal and produces a high-frequency low-resolution (usually 1-b) output word. The modulator shapes the quantization noise in the baseband and pushes it out to higher frequencies. The digital decimator acts as a low pass filter to remove the quantization noise and produces the digital high resolution word at Nyquist rate. The area and power budget per channel of conventionally designed oversampled analog-to-digital converters has precluded their application from areas where a large number of low frequency signals need to be converted simultaneously. A new oversampled A/D design methodology is proposed to significantly cut the power and area budget per channel of an oversampled analog-to-digital converter [4]. The design and implementation of a 16-channel, 14-b per channel oversampled analog-to-digital converter for multichannel applications is presented.

II. System Level Design Methodology

In a conventional design of an oversampled A/D, the total number of data channels going through the decimator is equal to the number of channels going through the modulator [5]. This practice is the result of viewing the oversampled A/D as a cascade of a modulator and a decimator block. In order to use the oversampled converters for processing very large number of channels simultaneously, we propose to optimize the analog and digital portions of the system separately. The *Multichannel Oversampled Data Acquisition System* (MODAS) is shown in Fig. 1. The output of the sensors is fed into an analog front end chip which contains N modulators working in parallel. The single bit output of each of the modulators is time multiplexed onto a single digital line which is fed into the multichannel decimator handling the output of M analog modulators. The number of channels N processed by the analog front end does not have to be equal to the number of channels M processed by the digital decimator. The two parts of the system are optimized separately to maximize the number of channels processed per chip. This system level partitioning of the two parts of an oversampled converter maximizes the use of silicon to convert the analog signals into a digital format at the front end of the system. The single-bit digital representation can then be routed to the digital decimator without the fear of corrupting the signal. This block diagram makes two assumptions: The first is that a very low power and small area modulator can be designed to meet the system specifications such that N of them can be placed on a single chip, and the second is that the decimator architecture has to be simplified to allow a highly multiplexed decimation system which could process M channels per chip. In the next section we will describe the *Extended Baseband Design* of the modulator which allows a very simple decimation structure per channel, thus making a highly multiplexed decimation structure feasible.

A. Extended Baseband Design

In the conventional design of oversampled analog-to-digital converters the baseband is defined to be the maximum input frequency of the analog signal. After the baseband of the signal is determined the modulator loop coefficients are chosen to minimize the integrated quantization noise in the baseband. The quantization noise energy rises sharply outside the baseband, requiring a very sharp cutoff for the decimation filter. The requirement of a very sharp cutoff and linear phase for the digital filter result in very large area and power consumption for the decimator block. For multichannel applications, a single stage FIR decimation algorithm lends itself naturally to a multiplexed and pipelined digital architecture. The single stage decimator makes use of single-bit manipulations and eliminates the need for digital multipliers. The order of an

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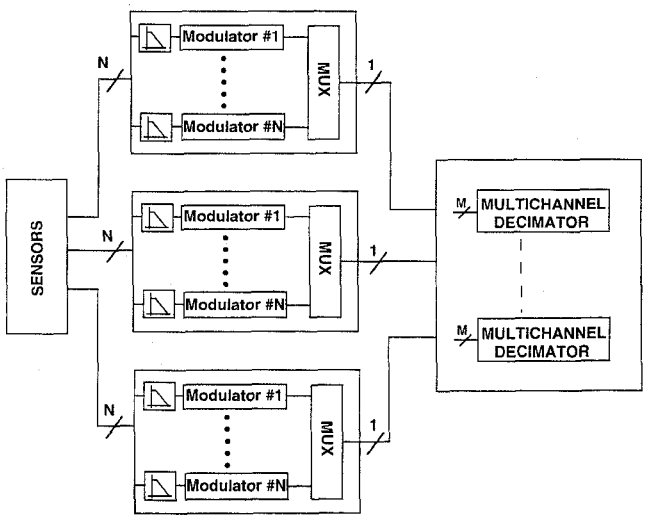

Fig. 1. Multichannel oversampled ADC architecture.

FIR filter can be predicted using the Kaiser estimate [6] if the baseband, transition width, and the sample rate are known. The formula for the Kaiser estimate is given below where δ_1 is the passband ripple, δ_2 is the stopband attenuation and Δf is the transition width.

$$(N-1) = \frac{-20\log_{10}\sqrt{\delta_1\delta_2} - 13}{14.6\Delta f}. \tag{1}$$

We can see that the transition width of the FIR filter is inversely proportional to the tap order of the filter for the required filter characteristics. This relationship can be exploited to reduce the tap order significantly by increasing the transition width of the FIR low pass characteristics. Consequently, the area per channel of a multichannel decimator architecture can be significantly reduced by increasing the transition width.

With the conventional definition of the modulator baseband as described above, the increase in transition width of the decimator characteristics implies that the sharply rising quantization noise outside the baseband would adversely contribute to the signal-to-noise ratio. This would result in a severe degradation in the performance of the modulator. This problem can be solved if the analog modulator baseband is increased to include the transition width of the decimator transfer function. This implies that the noise of the analog modulator must be shaped over an *extended baseband*. If the input signal bandwidth is F_i, then the modulator has to be designed for a baseband of $(F_i + \Delta f)$ where Δf is the part of the baseband used to relax the transition width requirement on the digital decimator block, as shown in Fig. 2.

The single loop N-th order modulator has N poles and N zeros in the system. For a given oversampling ratio and order the quantization noise is approximately given by [7];

$$n_0 = \frac{e_{\mathrm{RMS}}\pi^N(2f_0\tau)^{N+\frac{1}{2}}}{\sqrt{(2N+1)}} \tag{2}$$

$$e_{\mathrm{RMS}} = \frac{\Delta}{\sqrt{12}}. \tag{3}$$

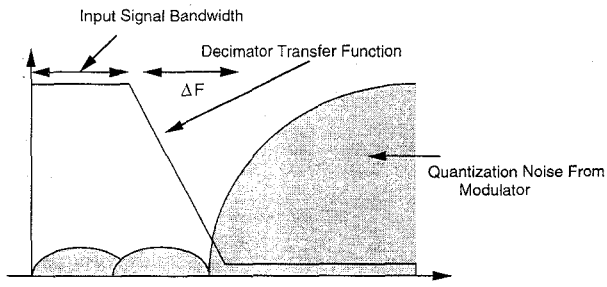

Fig. 2. Extended baseband design.

Where Δ is the stepsize of the quantizer, τ is the sampling clock period, f_0 is the baseband and N is the order of the modulator. The zeros in the transfer function can be placed within the baseband to optimally shape the quantization noise in the baseband [8]. If the baseband of the modulator is increased without increasing the order of the modulator, then the same number of zeros are required to suppress the quantization noise over a wider baseband, and thus the noise suppression is reduced. In order to maintain the signal-to-noise ratio and increase the baseband of the modulator, one must increase the order of the modulator. The decimator complexity is reduced by increasing the order of the front end modulator. This system level methodology requires that a higher order front end modulator can be designed to meet the area and power requirements for a multichannel parallel modulator array. The required specification for the intended application (digital mammography) is at least 12-b resolution over 1 kHz of baseband. The modulator was implemented with 7 kHz extended baseband and designed in such a way that the total integrated noise over the 8 kHz baseband meets the resolution requirement. The 7 KHz of extended baseband permits the use of a single stage decimation filter of 512 taps. This 512-tap single stage decimation filter can be used as the core of the highly multiplexed decimator architecture.

III. Low Power/Area Modulator Design

A. Power and Area Optimization for Modulator

The first step in the design of the modulator is to determine the power and area consumption of a modulator as a function of the signal baseband and resolution. This step determines the modulator order which minimizes the power dissipation and area while meeting the system specifications. A simple model is used to determine the power dissipation versus modulator order as a function of baseband and signal-to-noise ratio. In this modeling, a single loop modulator architecture was assumed.

The signal-to-noise ratio can be calculated as a function of the clock frequency and the modulator order for a given baseband as shown in (2). Thus, for a given signal-to-noise ratio and order we can calculate the minimum clock frequency required. The clock frequency of the system determines how fast the integrators must settle and is a measure of the power dissipated after modeling the integrator amplifiers.

The power dissipated in a modulator of order N has been modeled by assuming N identical integrator blocks. For now, the amplifier for each of the integrator blocks is modeled as a fully differential class A amplifier. However, it will be shown later that the type of the amplifier, class A or AB, makes little difference. The minimum current required in the integrator is a function of slewing and linear settling requirements, and we need to model both to determine the dominant process. To model the slewing requirements on the amplifier we assumed the maximum output swing of the integrator blocks to be one fifth of the supply voltage, and the maximum amplifier slewing time to be one eighth of the clock period. These assumptions and models resulted in the amplifier output current to be:

$$\Rightarrow I_{\text{out}} = \frac{8C_L V_{\text{supp}} f_s}{5}. \tag{4}$$

This gives us an upper limit on the bias current required in the output leg of a class-A amplifier to meet the slewing requirements with a capacitive load C_L. The linear amplifier settling was modeled by assuming that the amplifier had to settle within one eighth of the clock cycle and needed five time constants to settle. The time constant is related to the unity gain frequency but in switched capacitor implementation the amplifier's feedback gain is determined by:

$$M = \frac{C_s + C_i}{C_i} \tag{5}$$

which is not unity. This reduces the effective settling bandwidth of the amplifier and the reduction factor is called M. For a class-A amplifier:

$$\omega_0 = \frac{g_m}{C_L} \tag{6}$$

and for MOS applications,

$$g_m = \frac{I_t}{V_{\text{gs}} - V_{\text{th}}} \tag{7}$$

where I_t is the tail current for the input differential pair. Substituting this expression in the unity gain expression and using the above mentioned assumptions of five timeconstants within one eighth of the clock period we arrive at the expression for the minimum required tail current of the input differential pair.

$$I_t = 40\ MC_L f_s (V_{\text{gs}} - V_{\text{th}}). \tag{8}$$

Assuming $((V_{\text{gs}} - V_{\text{th}}) \approx 0.5$ V), the current requirement for the linear settling component is greater than the slewing criteria. Thus we use the minimum current requirement dictated by the linear settling criteria to model the current of the integrator, so that a class A or AB amplifier has the same criterion.

The total current in the amplifier can be represented as β times this value where β is a function of the topology of the amplifier. For an N-th order modulator there would be N amplifiers in the loop and thus we would have to multiply the single amplifier current estimate by N. The total modulator power can be given by:

$$\text{Modulator Power } = 40\ MC_L f_s (V_{\text{gs}} - V_{\text{th}}) N \beta V_{\text{supp}}. \tag{9}$$

This simple model gives us an expression for the complete power dissipation in an N-th order modulator. The value of the load capacitance C_L is calculated using the kT/C noise criteria for the required resolution. The capacitance is a function of both the required resolution and the oversampling ratio. Assuming a full scale input signal of 1 V, the minimum capacitance from thermal noise criteria can be given by:

$$C_L = 10^{\frac{\text{res}}{10}} kT \frac{2f_0}{f_s} \tag{10}$$

where res is the resolution in dBs, f_0 is the signal baseband and f_s is the sampling frequency. The values of constants $\beta, V_{\text{supp}}, M$ and $(V_{\text{gs}} - V_{\text{th}})$ in (9) can be chosen according to system specifications. For our system we used $\beta = 2, V_{\text{supp}} = 5.0$ V, $M = 2$ and $V_{gs} - V_{\text{th}} = 0.5$ V. If we substitute these values in (9) we get:

$$\text{Modulator Power } = 80\ f_s C_L N V_{\text{supp}}. \tag{11}$$

Substituting the expression for capacitance derived from the thermal noise criteria we get:

$$\text{Modulator Power} = 80(10^{\frac{\text{res}}{10}}) kT(2f_0) N V_{\text{supp}}. \tag{12}$$

This gives us a fundamental limit on the modulator power dissipation as function of resolution, baseband and order. This shows that power is independent of the sampling frequency and is linearly dependent on order of the modulator for a given resolution and baseband if the minimum capacitance estimate from thermal noise limit is used. In the derivation of this model we assumed all integrators of the modulator to be identical. In a practical implementation of a modulator optimized for power, the second and higher stages do not have to use the capacitor value dictated by the thermal noise limit. The second and higher order integrator blocks can use a minimum value of the capacitance. The loop coefficients of a higher order loop are determined by the ratio of sampling to integrating capacitors and this can place a lower limit on the integrating capacitor. The smaller of the two capacitance values, the thermal noise estimate and the minimum capacitance limit, determine the first integrator capacitance. Second and higher order stages use the minimum capacitance. This model is given by:

$$\begin{aligned}\text{Modulator Power } &= 80(10^{\frac{\text{res}}{10}}) kT(2f_0) V_{\text{supp}} \\ &\quad + 80 f_s C_{\min} (N-1) V_{\text{supp}}.\end{aligned} \tag{13}$$

This model of the modulator power dissipation was used to plot the power dissipation versus order as a function of basebands and signal-to-noise ratios shown in Fig. 3 and 4. In our simulations we used 0.5 pF as the minimum capacitance value. The calculations show that the power versus order is a function of the signal-to-noise ratios. For higher resolutions the first stage capacitance is significantly higher than the minimum capacitance, which results in very small effect from increasing modulator orders. Whereas for lower resolutions all the stages are using minimum capacitance value and thus a stronger dependence on order is seen. For our implementation we decided to use identical integrator blocks to minimize design time. For identical integrator blocks the same curves can be plotted and they showed the third order to have a distinct minimum for 90 dB resolution [9]. Thus we used the third order architecture for our modulator design.

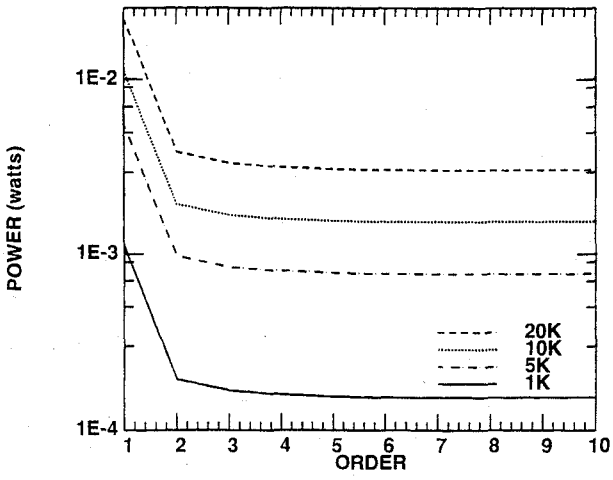

Fig. 3. Power dissipated versus order as a function of basebands; basebands 1 K, 5 K, 10 K, 20 K; SNR = 100 dB; $C_{\min} = 0.5$ pF.

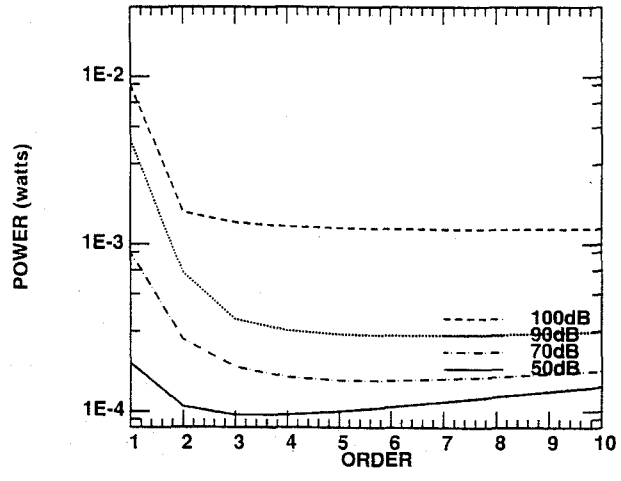

Fig. 4. Power dissipated versus order as a function of resolution; basebands 8 K, SNR = 100 dB, 90 dB, 70 dB, 50 dB; $C_{\min} = 0.5$ pF.

B. Modulator Architecture

Fig. 5. shows the block diagram of the third order single loop analog modulator with distributed feedback where the output of the single-bit quantizer is fed back to the input of each of the three integrators in the loop [10]. The loop coefficients (A_i) and (B_1) determine the pole locations. The coefficient B_1 determines the complex zero pair location in the baseband, while one real zero is at dc. The architecture chosen does not require an active summer at the input and has also been referred to as the "cascade of resonators" structure [10]. The feedback around the second and the third integrator forms the resonator structure. The complex transmission zeros in the quantization transfer function can be designed by selecting the correct resonator frequency. This topology has superior high frequency settling properties because the integrators and resonators are connected without the delay-free loops and the worst case settling happens when two amplifiers settle in series. The errors resulting from this worst case settling

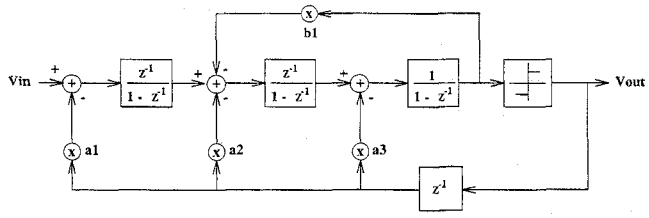

Fig. 5. Third order Delta-Sigma modulator.

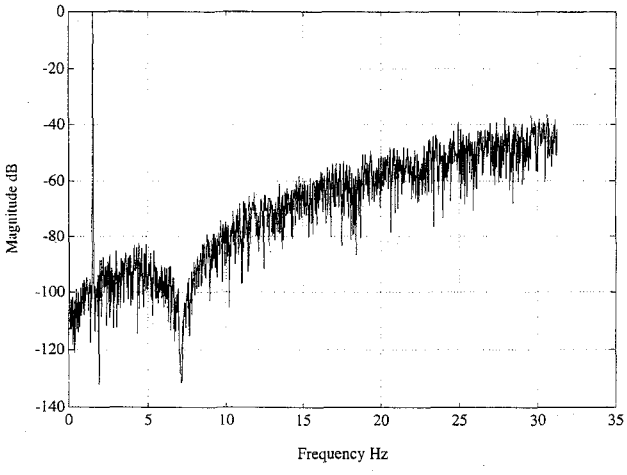

Fig. 6. Simulated modulator output with opamp gain of 1000.

only disturb the relative positioning of the noise shaping transmission zeroes for which the architecture is shown to be insensitive over a wide range [11]. The distributed nature of the quantized feedback improves the stability characteristics of the loop even with one or more integrators in saturation.

The system function for the topology in Fig. 5 is derived by replacing the integrators with their discrete-time-equivalents and by modeling the in-loop ADC as an additive white noise source $E(z)$ [12]. Each of the integrators is modeled as:

$$H(z) = \frac{K_i z^{-1}}{1 - z^{-1}} \tag{14}$$

where K_i is the gain of the i-th integrator. The resulting system function can be expressed as a combined response to the input $X(z)$ and the quantization noise $E(z)$,

$$Y(z) = H_x(z)X(z) + H_E(z)E(z) \tag{15}$$

where

$$H_X(z) = \frac{K_1 K_2 K_3 z^{-2}}{1 + \alpha_2 z^{-1} + \alpha_3 z^{-2} + \alpha_4 z^{-3}} \tag{16}$$

$$H_E(z) = \frac{(1 - z^{-1})(1 - (K_2 K_3 B_2 - 2)z^{-1} + z^{-2})}{1 + \alpha_2 z^{-1} + \alpha_3 z^{-2} + \alpha_4 z^{-3}} \tag{17}$$

and $\alpha_i s$ are given by:

$$\alpha_2 = ((-B_2 K_2 - a_3)K_3 - 3)$$
$$\alpha_3 = (((B_2 - A_2)K_2 + 2A_3)K_3 + 3)$$
$$\alpha_4 = ((A_2 - A_1 K_1)K_2 - A_3)K_3 - 1.$$

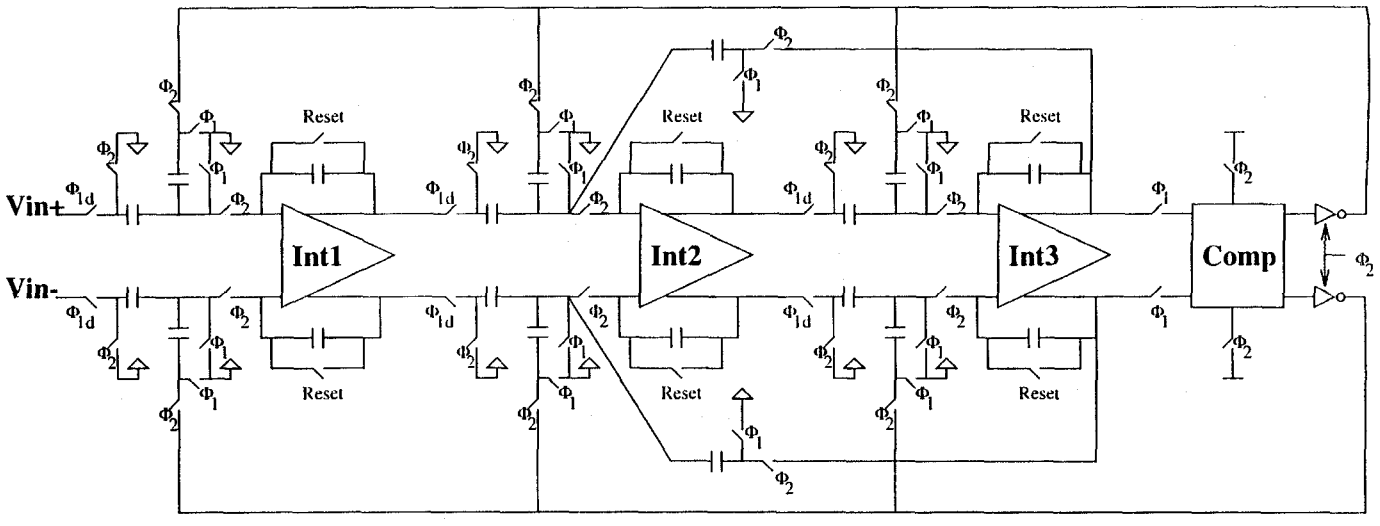

Fig. 7. Switched capacitor implementation of third order modulator.

The system function poles are determined both by the A and the B coefficients whereas the complex zero location is only a function of the resonator frequency which is determined by B_1. Elliptic filter design was used to determine the loop coefficients. Fig. 6 shows the simulated output spectrum of the modulator with the opamp gain of 1000.

The switched capacitor circuit implementation of the third order modulator is shown in Fig. 7. The basic circuit block for the implementation of the delta-sigma modulator is the switched capacitor integrator. A fully differential topology was chosen to minimize channel to channel crosstalk in a multichannel chip and to improve the power supply and common mode noise rejection. The switched capacitor implementation uses two nonoverlapping clocks Φ_1 and Φ_2. In the implementation of this circuit, the clock controlling the switch between the input signal and the sampling capacitor is a delayed version of the first phase clock and is shown as Φ_{1d} in Fig. 7. This is referred to as *clock sliding* and is done to minimize the signal dependent charge injection from the switch onto the sampling capacitor. Ideally the switches feeding the quantized feedback signal into the integrator block should also have the clocks delayed, but it was not used in this design to minimize area and power consumption.

C. Operational Amplifier Design

The most important criteria for the design of this amplifier are area and power dissipation. The topology must meet the settling time requirements within half the clock period while minimizing power.

The opamp topology [13] chosen is shown in Fig. 8. The fully differential input signal is applied to the input transistors $M1$ and $M2$ which are cross coupled with $M3$ and $M4$. The transistors $M5$–$M7$ and $M6$–$M8$ are used to provide $V_{\text{in}+}$ and $V_{\text{in}-}$ to $M3$ and $M4$ respectively with a dc offset to bias them appropriately. The reference current source I_{ref1} sets the dc bias current through $M5$–$M7$ and $M6$–$M8$ legs. The switched capacitor common mode feedback is used to control the common mode level at the output of the amplifier. The capacitors $C1$ and $C2$ connected between the drain and gates of transistors $MCM4$ and $MCM3$ are used to sense the common model level.

TABLE I
SIMULATED OPAMP SPECIFICATIONS

Parameter	Value
Open Loop Gain	71 db
Unity Gain Bandwidth	2 MHz
CMRR (±5% Mismatch)	83 db
Positive PSRR (±5% Mismatch)	65 db
Negative PSRR (±5% Mismatch)	48 db
Output Swing	± 2V
Power Dissipation	0.29 mW
Supply Voltages	± 2.5V

This topology is essentially single gain stage design. A reasonable gain (≈ 3000) is required to achieve good power supply and common mode rejection and linearity for the amplifier. The cascode transistors were not used in the output stage to improve the gain of the amplifier since the total area and power consumption cost of adding the cascode transistors were not acceptable. Very long channel lengths of the output transistors were employed to achieve high output resistance. Table I shows the simulated specifications of the amplifier in the switched capacitor integrators for the third order modulator.

D. Comparator Design

The quantizer in the third order modulator loop is a single-bit comparator [14]. The comparator is a fully differential circuit which determines the sign of the input signal and produces a digital output. Fig. 9 shows the circuit schematic of the single-bit comparator used in the design. The sensitive node which samples the input charge is buffered from the following circuitry through the clocked inverters on either side. The most important part of the quantizer is the reference voltages

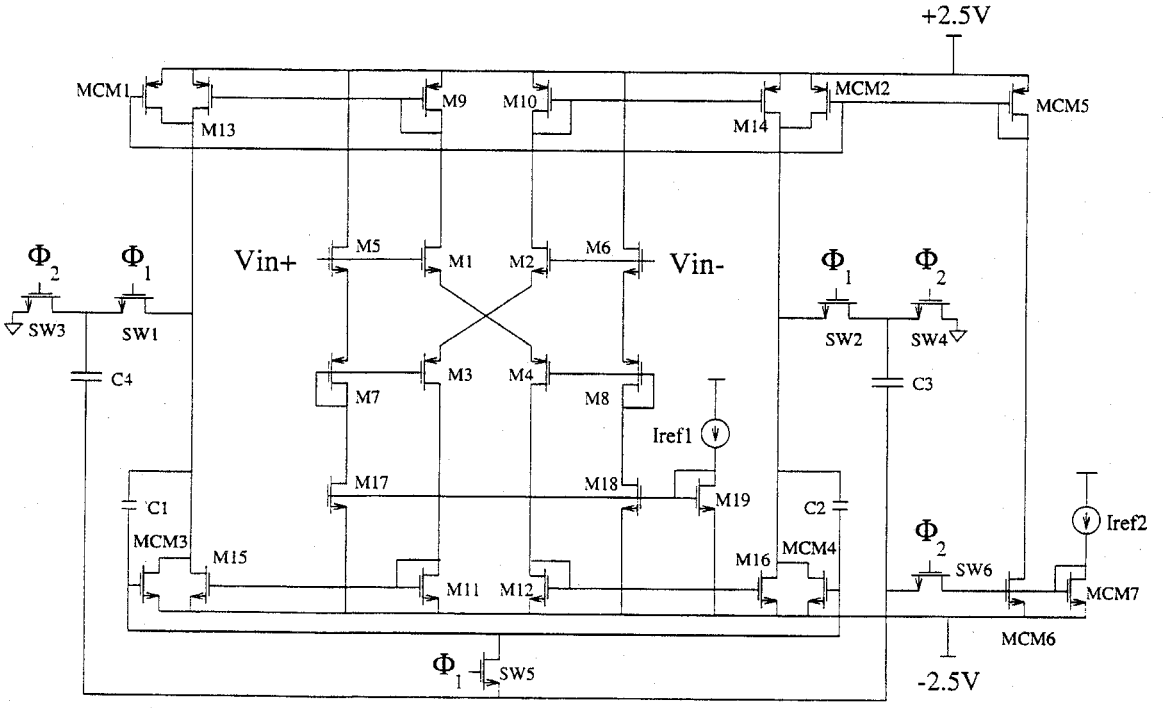

Fig. 8. Fully differential operational amplifier circuit.

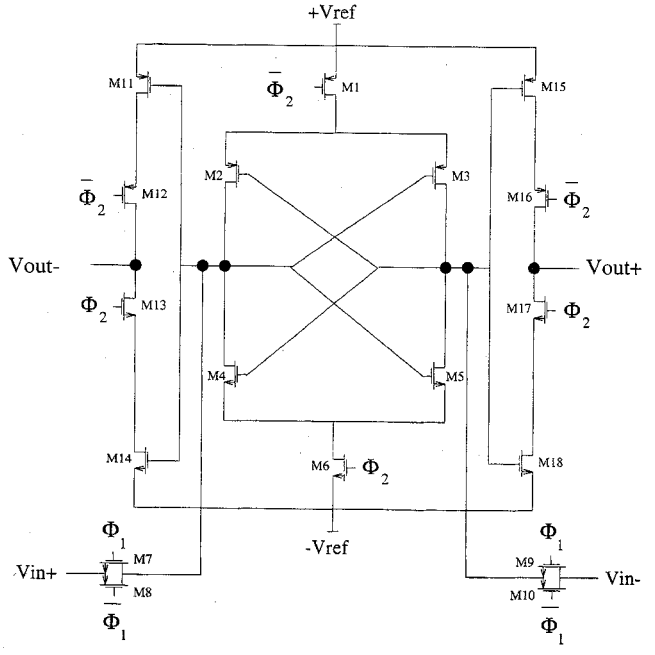

Fig. 9. Fully differential comparator circuit.

since they determine the noise contribution to the input signal through the feedback path. The noise on the output of the DAC becomes indistinguishable from the input signal and degrades the modulator performance significantly. Separate clean supplies are used for the DAC reference voltage.

E. Multiplexer Circuit

Fig. 10 shows the two stages of the 16-channel multiplexing circuitry, This is a parallel load and serial shift single bit

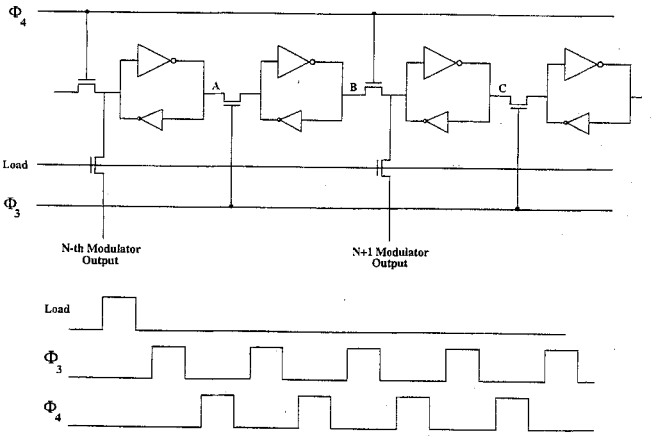

Fig. 10. Multiplexing circuitry for 16-channel ADC.

registers that load the output of all the modulators in parallel and then shift it out one bit at a time on the single line. When the load signal goes high, the clocks Φ_3 and Φ_4 are low. On the load signal the outputs of all the modulators drive the register input and the inverted output appears at nodes A and C. After the parallel load, the load signal goes low and the clocks Φ_3 and Φ_4 shift the bits serially such that the signal at A appears at B after the first pulse of Φ_3 and appears at C after the first pulse of Φ_4, and so on down the line. The load signal appears at the modulator clock rate of 500 KHz. The shift register clocks are 16 times faster and thus the output data rate of the time multiplexed signal is 8 MHz.

IV. Measurement Results

The 16-channel analog-to-digital converters were fabricated in a 2μ double poly CMOS process and the die photo is

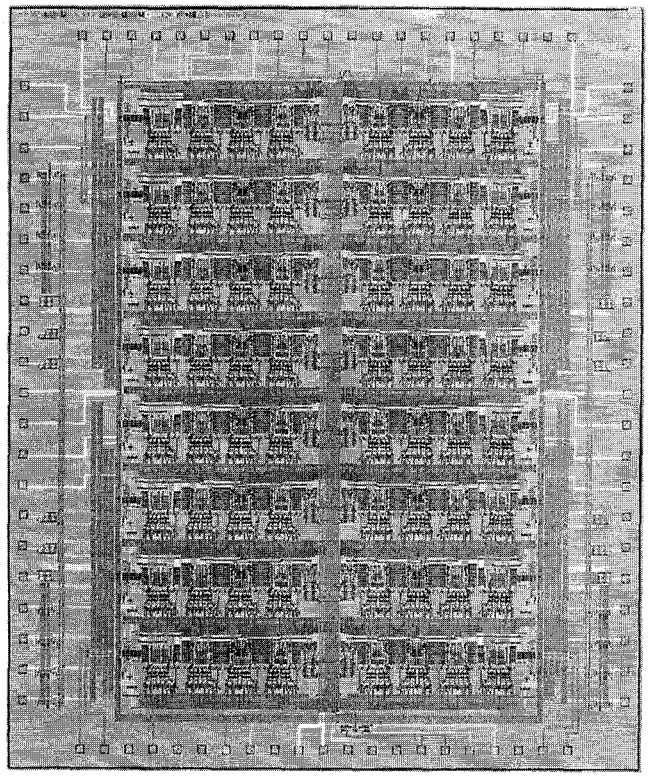

Fig. 11. The die photo of 16-channel oversampled A/D.

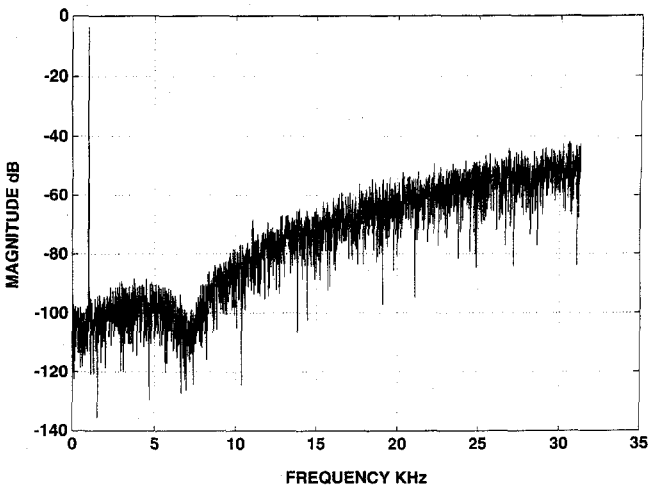

Fig. 12. Measured FFT plot of 999.45 Hz sine-wave input with a 500 KHz sampling rate.

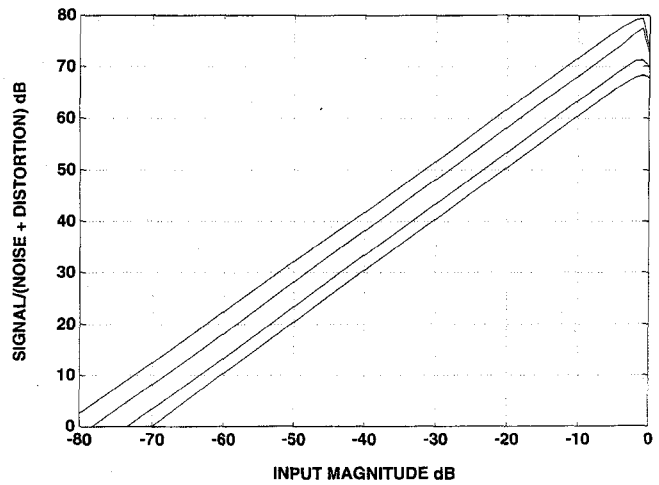

Fig. 13. Measured SNDR curves for 1 K, 2 K, 4 K and 8 K basebands.

shown in Fig. 11. Each of the channels has an application specific preamplifier at the input. The chips were characterized in two steps. First, a single oversampled modulator was characterized by itself with differential voltage inputs with all the circuits running on the 16-channel test chip. Fig. 12 shows the measured output spectrum of a sine wave input at a frequency of 999.45 Hz, and the modulator was being clocked at its full design speed of 500 KHz. The FFT plots are normalized to the full scale input voltage for which the modulator is stable which is -6 dB of the DAC reference voltage. The performance is limited by the quantization noise and not the thermal or $1/F$ noise because the measurement clearly shows the quantization noise in the baseband is shaped and rises sharply out of the baseband of 8 KHz. Fig. 13 shows the signal-to-noise plus distortion curves as a function of the input signal magnitude. The performance of the modulator is limited by the third harmonic distortion at higher magnitudes. The sliding clocks were used only for the input signal to the integrator and not for the feedback signals which could be a reason for the distortion at higher magnitudes due to signal dependent charge injection. Lower order modulators have suffered from tones in the baseband for certain dc inputs to the modulator. Fig. 14 shows the measured idle channel noise plot as a function of the dc input bias voltage where the noise is integrated over the full 8 KHz baseband. Several very closely spaced data points were taken around exact fractions of the DAC reference voltage to observe tones in the baseband but as can be seen from the plot no tones were visible.

On any multichannel system crosstalk is an important performance criteria. The 16-channel MODAS chip was tested with several different input configurations to identify the worst case. The worst case crosstalk was measured by applying full scale input signals of 2 KHz and 1.6 KHz to the two channels and the inputs to the two adjacent channels were provided with dc inputs. Fig. 15 shows the output spectrum of the channel with dc input and the 2 KHz and 1.6 KHz signal coupling from the adjacent channels can be observed rising out of the baseband. The crosstalk measure was defined as the ratio of the full scale signal input to the peak of the crosstalk tone measured in the baseband. The performance summary of the 16-channel analog-to-digital converter is presented in Fig. 16.

V. Conclusion

A new design methodology was presented to introduce oversampled analog-to-digital converters for multichannel signal acquisition systems. A 16-channel oversampled analog-to-digital converter with 14-b of resolution over 1 KHz of baseband per channel was designed and built to demonstrate the feasibility of the proposed approach. The extended base-

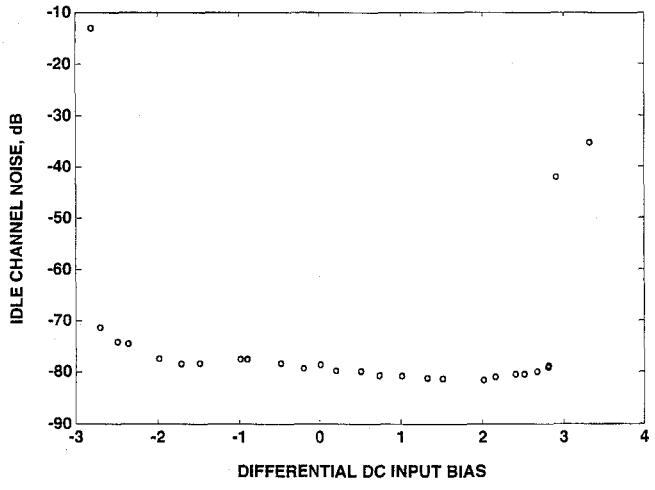

Fig. 14. Measured idle channel noise versus input dc bias for 8 KHz baseband.

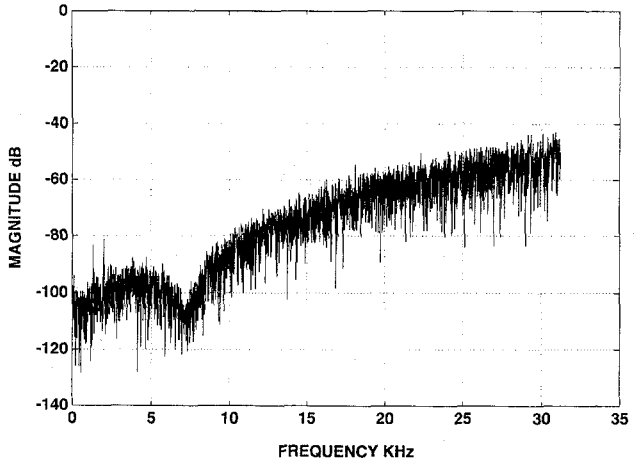

Fig. 15. Crosstalk measurement with dc inputs applied to the channel.

Parameter	Value
SNR (1 KHz)	84.4 db
SNR (8 KHz)	69.2 db
SNDR (1 KHz)	79.9 db
SNDR (8 KHz)	68.9 db
Cross Talk	-80 db
Clock Frequency	500 KHz
Max. Input Voltage	5V (differential)
Max. Input Current	$10\mu A$
Power Per Channel	0.94mW
Area Per Channel	2mm x 1mm
Power Supplies	$\pm$ 2.5V
IC Dimensions	7.5mm x 8.5mm
Process	5V, 2μm, Double Poly CMOS

Fig. 16. Performance summary of 16-channel ADC.

band concept used for the design of the modulator reduces the complexity of the modulator and allows for the multiplexing of a large number of modulator outputs. The higher order modulator does not necessitate increased complexity in the decimator structure. Very efficient hardware can be used to implement the relaxed transition width single stage FIR decimator provided higher output rate can be tolerated in the application and it is not obvious that the increased output rate versus the hardware complexity saving would result in net increased power. The overall power optimization of the digital decimator and modulator was beyond the scope of this work. The test results show that in spite of the large number of channels, the noise and crosstalk can be controlled to within the required specifications.

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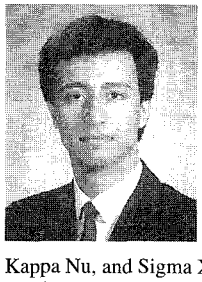

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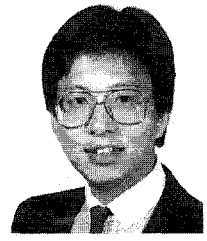

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