

Special Papers

A Self-Calibrating 15 Bit CMOS A/D Converter

HAE-SEUNG LEE, STUDENT MEMBER, IEEE, DAVID A. HODGES, FELLOW, IEEE,
AND PAUL R. GRAY, FELLOW, IEEE

Abstract—A self-calibrating analog-to-digital converter employing binary weighted capacitors and resistor strings is described. Linearity errors are corrected by a simple digital algorithm. A folded cascode CMOS comparator resolves 30 μV in 3 μs . An experimental converter fabricated using a 6 μm gate CMOS process demonstrates 15 bit resolution and linearity at a 12 kHz sampling rate.

I. INTRODUCTION

CONVENTIONAL successive-approximation analog-to-digital conversion techniques require precise component matching to realize high resolution and linearity. Fast, high-resolution A/D converters usually have been realized in the form of hybrid circuits, where two or more different technologies can be combined for optimum performance. A complex thin-film resistor process and laser trimming are often used to provide necessary component matching. Mechanical stress during packaging and long term drift of laser trimmed components often pose serious problems for such converters.

In this paper, a self-calibration technique which enables a monolithic implementation of very high-performance analog-to-digital converters is described. This technique is based on a binary weighted capacitor array DAC [1], [2] and a resistor string DAC [3], [4]. During the calibration cycle, typically performed after each powerup, the ratio errors of the capacitors are measured and stored in a RAM. During the subsequent normal conversion cycles, these data are used to correct for the element matching errors of the capacitor array.

An A/D converter employing this technique can be implemented using standard CMOS or NMOS technology.

Manuscript received April 27, 1984; revised August 6, 1984. This research was supported in part by the National Science Foundation under Grants ECS-8023872 and ECS-8310442, and by the 1981-1982 State of California MICRO program with grants from Fairchild Semiconductor, Racal-Vadic, and GTE-Lenkurt.

H.-S. Lee was with the Department of Electrical Engineering and Computer Sciences and the Electronics Research Laboratory, University of California, Berkeley, CA 94720. He is now with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139.

D. A. Hodges and P. R. Gray are with Department of Electrical Engineering and Computer Sciences and the Electronics Research Laboratory, University of California, Berkeley, CA 94720.

Laser trimming is not needed. A major advantage of this technique is that no special fabrication technology is required, and no special trimming or testing equipment is needed. The calibration can be performed at any time without the use of external components. Any long term variation can be corrected by calibrating at appropriate intervals.¹

II. SELF-CALIBRATION TECHNIQUE

A block diagram of a self-calibrating A/D converter is shown in Fig. 1. This circuit consists of an N bit capacitor array *main DAC*, an M bit resistor string *sub DAC*, and a resistor string *calibration DAC*, which must have a few more bits of resolution than the sub DAC. Digital control circuits govern capacitor switching during the calibration cycle and store the nonlinearity correction terms in data registers. The ratio errors of the sub DAC, and overall quantization errors, accumulate during digital computation of error voltages. To overcome these errors for a 16 bit converter, 2 bits of additional resolution are needed during the calibration cycle.²

Fig. 2(a) shows an N bit weighted capacitor DAC. Suppose that each weighted capacitor C_n has a normalized ratio error of $(1 + \epsilon_n)$ relative to the ideal value due to process variations:

$$C_n = 2^{n-1}C(1 + \epsilon_n), \quad n = 1A, 1B, \dots, N. \quad (1)$$

The total linearity error consists of contributions from each capacitor ratio error. These contributions, *error voltages*, can be found to be

$$V_{\epsilon_n} = \frac{V_{\text{ref}}}{2^N} 2^{n-1} \epsilon_n \quad n = 1B, 2, \dots, N \quad (2)$$

where the subscript n corresponds to the capacitor C_n .

¹We have not observed any long-term drift in MOS capacitor ratios in the course of this work.

²In principle, one extra bit is adequate to achieve final linearity within 1 LSB of an ideal straight line, or within 1/2 LSB of an ideal staircase converter response. In practice, two extra bits are necessary to have a margin of safety.

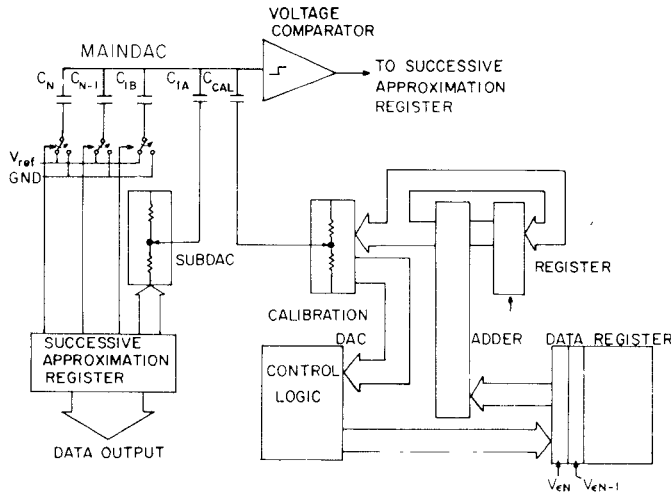


Fig. 1 Block diagram of self-calibrating A/D converter. Digital control logic amounts to a total of about 400 gates and 120 bits of RAM.

Then, the total linearity error V_{error} becomes

$$V_{\text{error}} = \sum_{i=1B}^N V_{\epsilon_i} D_i. \quad (3)$$

During the calibration cycle, individual error voltages V_{ϵ_n} 's are measured and digitized by the calibration DAC and then stored in the RAM. During the normal conversion cycle, the total error voltage V_{error} is computed by (3) in digital form, and converted to analog voltage by the same calibration DAC. This total error voltage is subtracted from the main DAC through the coupling capacitor C_{cal} to correct the initial linearity error.

The calibration cycle begins by measuring the error voltage due to the MSB capacitor C_N . This is done by sampling the reference voltage V_{ref} on all the capacitors except the MSB capacitor, as shown in Fig. 2(b). Next, charge is redistributed by reversing the switching configuration, as shown in Fig. 2(c). If the MSB capacitor is perfect, it will have exactly half of the total array capacitance. Thus, the top plate voltage is left unchanged by the charge redistribution. A ratio error in the MSB capacitor will cause a small change in the top plate voltage after the charge redistribution. This *residual voltage* V_{xN} is a direct measure of the error voltage corresponding to the error in the ratio of the MSB capacitance to the total array capacitance:

$$V_{xN} = 2V_{\epsilon N}. \quad (4)$$

Similarly, errors due to smaller capacitors are measured. In each case, a successive approximation search using the sub DAC is employed.

It can be shown easily that the general relation between residual voltages (V_{xn} 's) and the error voltages ($V_{\epsilon n}$'s) is

$$V_{\epsilon n} = \frac{1}{2} \left(V_{xn} - \sum_{i=n+1}^N V_{\epsilon i} \right), \quad n = 1B, 2, \dots, N-1. \quad (5)$$

This computation is performed in the digital domain by the

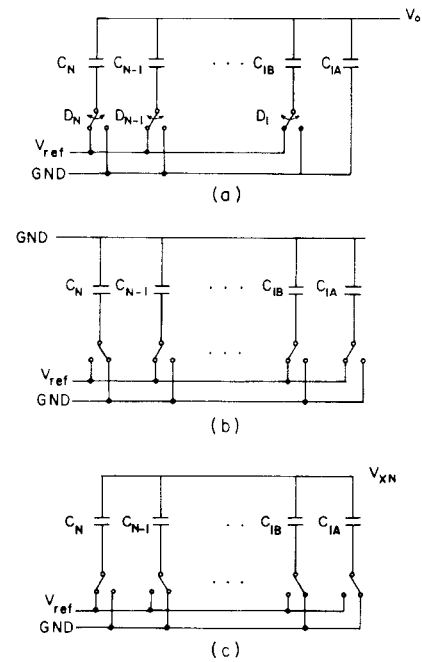


Fig. 2. Binary weighted capacitor array DAC. C_N is the largest capacitor; ideally it has half of the total array capacitance. C_{1A} and C_{1B} are the two smallest capacitors and are equal in value. (b) The self-calibration cycle begins with the MSB capacitor precharged to zero, while all other capacitors are charged in parallel to V_{ref} . (c) The top plate voltage V_{xN} (ideally zero) is a direct measure of error in the ratio of C_N to total array capacitance. Capacitors C_N through C_2 are evaluated by successive applications of this same process.

logic circuitry.

$$DV_{\epsilon N} = \frac{DV_{xN}}{2} \quad (6)$$

$$DV_{\epsilon n} = \frac{1}{2} \left(DV_{xn} - \sum_{i=n+1}^N DV_{\epsilon i} \right), \quad n = 1B, 2, \dots, N-1 \quad (7)$$

where $DV_{\epsilon n}$ and DV_{xn} stand for digitized error voltages (*correction terms*) and digitized residual voltages, respectively.

Therefore, by digitizing residual voltages using the sub DAC, correction terms $DV_{\epsilon N}$, $DV_{\epsilon N-1}$, ..., $DV_{\epsilon 1B}$ can be computed subsequently by (6) and (7) using a two's complement adder and a shift register. All these correction terms are stored in digital memory.

During subsequent normal conversion cycles, the calibration logic is disengaged. The converter works the same way as an ordinary successive-approximation converter, except that error-correction voltages are added or subtracted by proper adjustment of the calibration DAC digital input code. When the n th bit is being tested, corresponding correction term $DV_{\epsilon n}$ is added to the correction terms accumulated from the first bit (MSB) through the $(n-1)$ th bit. If the bit decision is 1, the added result is stored in the accumulator. Otherwise, $DV_{\epsilon n}$ is dropped, leaving the accumulator with the previous result. The content of the accumulator is converted to an analog voltage by the calibration DAC. This voltage is then subtracted from the main DAC output voltage through the capacitor C_{cal} . The overall operation precisely cancels the nonlinearity due to capacitor mismatches by subtracting V_{error} in (3)

from the main DAC. The only extra operation involved in a normal conversion cycle is one two's complement addition. For more detailed mathematical formulation of the self-calibration algorithm, refer to the earlier paper [5].

III. HIGH RESOLUTION COMPARATOR

To realize a fast, high-resolution A/D converter, a high-performance comparator is essential. For example, to achieve 16 bit resolution and at a 50 kHz conversion rate with ± 4 V reference voltages, the comparator should resolve $60 \mu\text{V}$ (1/2 LSB) in about 500 ns. During the calibration cycle, $15 \mu\text{V}$ resolution is needed to provide 18 bit digital resolution. However, a longer delay is permitted during the calibration cycle. Also, the effect of random noise in the comparator can be reduced by performing the calibration many times and averaging the results.

A two-stage amplifier is chosen for the comparator for easy offset cancellation. The amplifier section of the comparator should provide a gain of more than 100000 with the minimum delay possible and peak input referred noise less than $60 \mu\text{V}$.

When this amplifier is operated in the open-loop configuration, the dominant open-loop poles are determined by the parasitic capacitances at the high impedance nodes. The effect of large capacitive parasitics can be removed from the critical nodes by using cascode stages and source follower stages. A folded cascode amplifier (feasible in CMOS but not in NMOS) provides all the advantages of an ordinary cascode amplifier, while requiring less supply voltage. A schematic diagram of the amplifier employing a folded cascode input stage is shown in Fig. 3. Parasitic capacitances from the large input transistor $M1$ and $M2$ are isolated from the sensitive output nodes by the cascode transistors $M8$ and $M9$. Gate-to-source capacitance and Miller multiplied capacitance of $M6$ are decoupled by the source follower stage consisting of $M11$ and $M12$. A cascode circuit is used for the output stage for the same reason.

The effect of comparator offset voltage is cancelled by closing the feedback switch $M19$. However, charging the large DAC capacitor using only the bias current of the amplifier output stage would be very slow. To speed up the charging, a large switch $M20$ is added. This transistor brings the capacitor voltage to ground potential very quickly. After this switch opens, the offset voltage will be very small (several tens of millivolts at most), reducing the total time needed to settle to within 1/2 LSB of final value. After $M20$ is turned off and the capacitor voltage is at near ground, $M19$ is turned on, sampling the offset voltage on the capacitor. During this time the compensation capacitor C_c is connected to stabilize the amplifier. A 200 pF compensation capacitor would be needed for a 120 pF capacitor array load if the transconductances of the first and the second stages are comparable. A capacitor of this size is impractical for implementation on chip and would also severely limit the comparator slew rate and settling time.

A pole-zero cancellation technique is used to reduce the size of the compensation capacitor as well as to improve

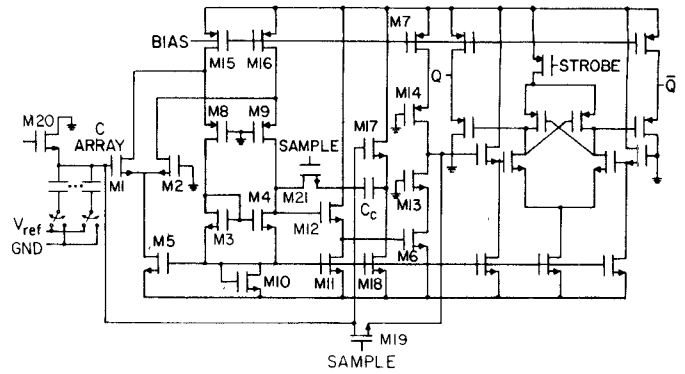


Fig. 3. Folded cascode CMOS comparator with high-speed latch. Input stage includes $M1-M4$, $M8$, $M9$, while $M11$, $M12$ form a level shifter. Output stage is made up of $M6$, $M7$. Unnumbered devices form a strobed output latch with sensitivity of about 100 mV.

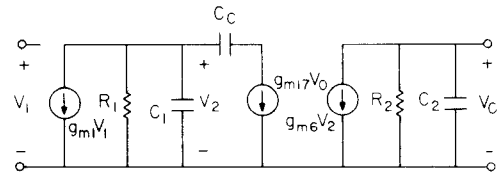


Fig. 4. Equivalent circuit of closed-loop comparator. C_1 is the parasitic capacitance and the drain of $M9$; C_c is the compensation capacitor; C_2 is the load capacitance at the drain of $M13$.

closed-loop performance. A left half-plane zero is introduced by the source follower stage consisting of $M17$ and $M18$. This zero is located so as to cancel the nondominant pole.

Consider the simplified equivalent circuit of Fig. 4. In this equivalent circuit, the common gate stage of $M8$ and $M9$, as well as the source follower stage of $M11$ and $M12$, are omitted since the poles and zeros associated with these stages lie well beyond the range of interest. C_1 is the parasitic capacitance at the output of the first stage (drain of $M9$) and C_2 represents the load capacitance at the drain of $M13$. The node voltage equations for this equivalent circuit are

$$gm_1 V_1 + \left(\frac{V_2}{R_1} + sC_1 \right) V_2 + \frac{sC_c}{1 + s \frac{C_c}{gm_{17}}} (V_2 - V_o) = 0 \quad (8)$$

$$gm_6 V_2 + \left(\frac{1}{R_2} + sC_2 \right) V_o = 0. \quad (9)$$

Solving for V_o/V_1

$$\frac{V_o}{V_1} = - \frac{a}{1 + bs + cs^2 + ds^3} \left(1 + s \frac{C_c}{gm_{17}} \right) \quad (10)$$

where

$$\begin{aligned} a &= gm_1 gm_6 R_1 R_2 \\ b &= R_1 (C_1 + C_c) + R_2 C_2 + gm_6 R_1 R_2 C_c + \frac{C_c}{gm_{17}} \\ c &= R_1 R_2 C_2 (C_1 + C_2) + \frac{C_c}{gm_{17}} (R_1 C_1 + R_2 C_2) \\ d &= \frac{R_1 C_1 C_c R_2}{gm_{17}} \end{aligned}$$

Assuming that the poles are widely spread and that $C_c, C_2 \gg C_1, R_1, R_2 \gg 1/gm_{17}$,

$$p_1 = -\frac{1}{gm_6 R_1 R_2 C_c} \quad (11)$$

$$p_2 = -\frac{gm_6}{C_2} \quad (12)$$

$$p_3 = -\frac{gm_{17}}{C_1} \quad (13)$$

$$z = -\frac{gm_{17}}{C_c} \quad (14)$$

To eliminate the nondominant pole p_2 , we require that

$$z = p_2 \quad (15)$$

or

$$\frac{gm_{17}}{gm_6} = \frac{C_c}{C_2} \quad (16)$$

To provide a 60° phase margin at the unity gain frequency ω_1 , the compensation capacitor should be selected such that

$$\frac{p_3}{\omega_1} = \tan^{-1} 60^\circ = \sqrt{3} \quad (17)$$

or

$$\frac{gm_6 C_c C_c}{gm_1 C_1 C_L} = \sqrt{3} \quad (18)$$

The major component of C_1 is the junction capacitance between the compensation capacitor bottom plate and the substrate. Our capacitors were formed between polysilicon and n^+ diffusion into the substrate. Using the measured value for the zero-bias $n^+ - p$ junction capacitance $C_{j0} = 0.64 \times 10^{-4}$ pF/ μm^2 , $\phi = 0.8$ V and junction reverse bias $V_a = 3$ V.

$$C_j = \frac{C_{j0}}{\sqrt{1 + \frac{V_a}{\phi}}} = 3 \times 10^{-5} \text{ pF}/\mu\text{m}^2.$$

For a 1000 Å capacitor dielectric oxide, C_{ox} is

$$C_{\text{ox}} = 3.45 \times 10^{-4} \text{ pF}/\mu\text{m}^2.$$

Thus,

$$\frac{C_c}{C_1} = \frac{C_{\text{ox}}}{C_j} \approx 9.$$

Using this value, (18) becomes

$$\frac{C_c}{C_L} \approx 0.2 \frac{gm_1}{gm_6}.$$

For $gm_1 \approx gm_6$ and $C_L = 120$ pF:

$$C_c = 24 \text{ pF}.$$

Compared with 200 pF required for the simple pole-splitting compensation, this is a great reduction.

The transconductances of n-channel transistors $M8$ and $M17$ should be scaled in proportion to the ratio between the compensation capacitor and the array capacitor. The transconductances of transistors may be scaled by scaling the aspect ratio. The transconductances of $M6$ and $M17$ are

$$gm_6 = \left\{ 2K \left(\frac{Z_6}{L} \right) I_{D6} \right\}^{1/2} \quad (19)$$

$$gm_{17} = \left\{ 2K \left(\frac{Z_{17}}{L} \right) I_{D17} \right\}^{1/2} \quad (20)$$

The drain current of $M17$ is

$$I_{D17} = I_{D18} = \frac{K}{2} \left(\frac{Z_{18}}{L} \right) (V_{GS18} - V_T)^2. \quad (21)$$

Thus,

$$\begin{aligned} gm_{17} &= \left\{ K^2 \left(\frac{Z_{18}}{L} \right) \left(\frac{Z_{17}}{L} \right) (V_{GS18} - V_T)^2 \right\}^{1/2} \\ &= K (V_{GS18} - V_T) \left(\frac{Z_{17}}{L} \right)^{1/2} \left(\frac{Z_{18}}{L} \right)^{1/2}. \end{aligned} \quad (22)$$

Since $V_{GS8} - V_T = V_{GS18} - V_T$ for $V_i = 0$,

$$\frac{gm_{17}}{gm_6} = \frac{\left(\frac{Z_{17}}{L} \right)^{1/2} \left(\frac{Z_{18}}{L} \right)^{1/2}}{\left(\frac{Z_6}{L} \right)}. \quad (23)$$

Assuming $M17$ and $M18$ are identical,

$$\frac{gm_{17}}{gm_6} = \frac{\left(\frac{Z_{17}}{L} \right)}{\left(\frac{Z_6}{L} \right)} = \frac{Z_{17}}{Z_6}. \quad (24)$$

This equation shows that the ratio of the transconductances can be scaled by directly scaling the widths of the two transistors. In reality, due to the different body bias, the transconductances of $M6$ and $M17$ cannot match precisely. The result of the mismatch will be a slow settling component in the transient response [6]. The initial amplitude of the slow settling component can be shown to be

$$V_{SS}(0) = V_i \frac{\Delta\omega}{\omega_1} \quad (25)$$

where $V_{SS}(0)$ is the initial amplitude of the slow settling component, V_i is the input voltage, $\Delta\omega$ is mismatch between the pole and the zero locations, and ω_1 is the unity gain bandwidth of the amplifier. The input voltage V_i is the offset voltage of the comparator plus the charge injection from the big grounding switch, which will not exceed 100 mV. Assuming 20 percent mismatch of transconductances and unity gain frequency $\omega_1/2\pi$ of 4 MHz, the initial amplitude of the slow settling component is less than 2

mV. Approximately 5 time constants of the slow settling component would be required to attain less than 20 μ V error. SPICE simulations shows that 1.5 μ s is needed for the amplifier to settle within 20 μ V of the final value. This is acceptable because the loop is closed only once per 20 μ s conversion interval.

The closed loop offset sampling does not provide complete offset cancellation due to the charge injection from the small feedback switch *M19*. This residual offset voltage is related to the gate overlap capacitance C_{OL} , the gate area of the switch WL and the voltage levels applied to the gate

$$\Delta V_{OS} = -\frac{C_{OL}}{C_{TOT}}(V_T - V_{GS}(\text{OFF})) - \frac{WLC_{ox}}{2C_{TOT}}(V_{GS}(\text{ON}) - V_T). \quad (26)$$

This residual offset voltage for the prototype converter was measured to be about 1.2 mV. This offset voltage is constant as long as the voltage levels are reasonably constant. A 200 mV drift in the threshold voltage V_T or gate-to-source voltages $V_{GS}(\text{ON})$ and $V_{GS}(\text{OFF})$ changes the offset voltage by only 40 μ V. The residual offset voltage can be digitized by the calibration DAC and stored in a RAM. This offset data can later be used for a simple digital correction of the residual offset voltage. Experimentally, the offset was reduced to less than 60 μ V after digital correction. A detailed description of the digital offset correction technique is presented in a separate paper [7].

The amplifier is followed by a high-speed latch as shown in the schematic diagram. The regeneration is activated by a *strobe* signal, which is applied between the clock edges by an analog delay circuit to avoid digital switching noise. A source follower stage is added between the amplifier and the latch to prevent feedthrough from the latch to the high-impedance output of the amplifier.

IV. EXPERIMENTAL RESULTS

The die photograph of the experimental chip is shown in Fig. 5. This chip contains a 10 bit plus sign capacitor array main DAC, a 5 bit resistor string sub DAC, and a 7 bit resistor string calibration DAC. The successive-approximation and control logic circuits are implemented off chip for simplicity and flexibility.

The capacitors are formed using a heavily doped polysilicon top plate and implanted bottom plate. n-type doping in both places is on the order of $10^{20}/\text{cm}^3$ in order to obtain a voltage coefficient of capacitance smaller than 20 parts per million per volt [8]. The array is made up of 1024 unit capacitors. The capacitance of the unit capacitor is defined by the polysilicon top plate which is $18 \times 18 \mu\text{m}$. The MSB capacitor is split into two identical halves and located at the sides of the array to reduce the effect of any possible gradient in etching or oxide thickness.

The resistor strings are formed by source-drain implantation of n-channel transistors. The size of the unit resistor is $20 \times 5 \mu\text{m}$. Tree decoders are included in both the sub

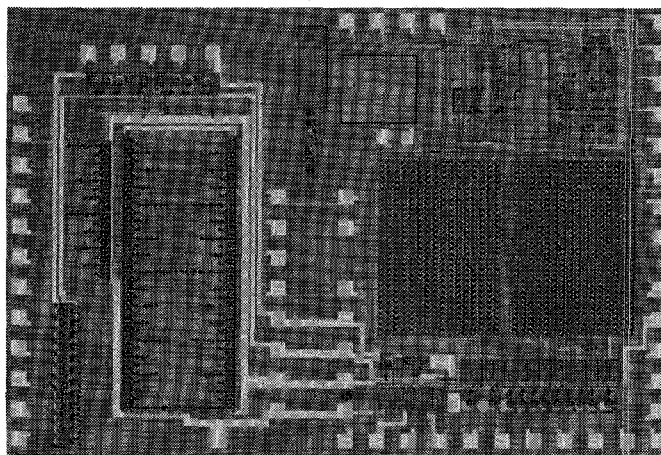


Fig. 5. Photograph of the die, fabricated at UC Berkeley. Overall chip dimensions are $2.8 \times 4.2 \text{ mm}$ in a $6 \mu\text{m}$ silicon-gate CMOS process.

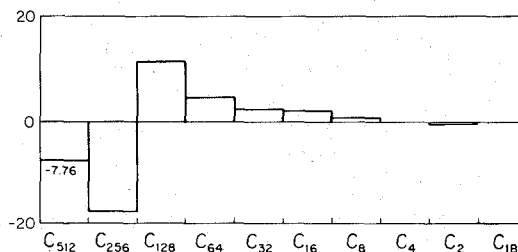


Fig. 6. Typical capacitor ratio error measured by the calibration circuits. Vertical axis is in unit of 1 LSB at the 16 bit level. The large error in C_{256} is due to a mask layout error.

DAC and the calibration DAC. To minimize mismatches due to possible contact resistance variations, contacts are avoided in the unit resistors. The interconnections between the resistors and the tree decoder are made in continuous n + material [2].

The total die area of the prototype chip excluding bonding pads is 7.5 mm^2 . A complete 16 bit converter with all the logic circuits would occupy about 15 mm^2 based on $5 \mu\text{m}$ design rules.

Fig. 6 shows a typical capacitor ratio error measured using the calibration circuits. To reduce the effect of random noise, each residual voltage is measured 16 times and the average value is used to compute the correction terms. The results are stated in terms of 1 LSB at a 16 bit level. As was shown in the previous section, each correction term is the direct measure of the ratio error. The ratio error shown in Fig. 6 corresponds to initial matching of a 9 bit plus sign. The large ratio errors of the larger capacitors were found to be systematic. We believe this is due to mask design which had varying etch widths for the polysilicon top plate. First-order cancellation of capacitor ratio errors due to etching effects can be obtained by use of design rules which provide equal-width etch channels around the perimeter of all unit capacitors.

A summary of the measured performance of the comparator is shown in Table I. The $3 \mu\text{s}$ worst-case delay is mainly the intentional timing delay between main DAC

TABLE I
MEASURED PERFORMANCE PARAMETERS OF COMPARATOR

Supply Voltages	± 5	V
Resolution	30	μV
Worst Case Delay	3	μs
RMS Input Referred Noise	20	μV
Power Dissipation	10	mW
Closed Loop Settling Time (to 20 μV , 120 pF Load)	1.5	μs
Die Area	0.65	mm^2

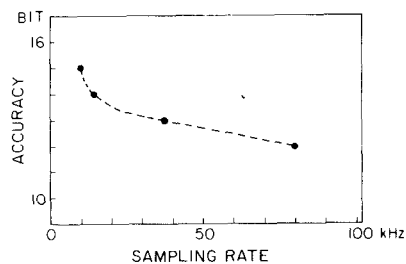


Fig. 7. Measured accuracy as a function of sampling rate for the experimental chip.

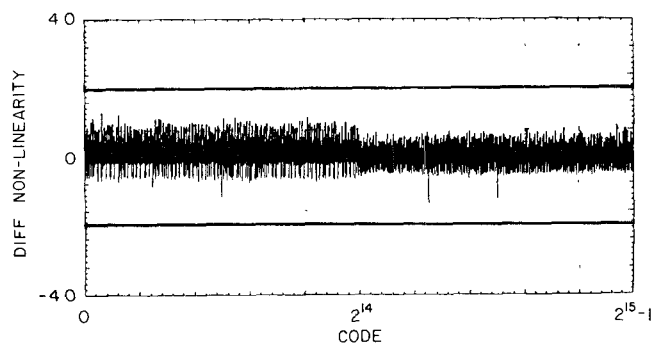


Fig. 8. Differential nonlinearity measured using a code-density test for the experimental converter operating at full speed.

switching time and the strobe time for the comparator output latch. Excessive digital switching noise was being coupled into the critical analog portion of the circuit. A delay of about 2.95 μs was deliberately introduced before strobing the latch to allow switching noise to decay to a sufficiently small level to achieve 15 bit conversion.

The speed-accuracy performance of the complete converter is shown in Fig. 7. 15 bit accuracy was obtained at 12 kHz sampling rate. Due to digital switching noise, the accuracy dropped down to 12 bits at 80 kHz sampling rate. Some of the switching noise may be coupled into the comparator via inductance (~ 10 – 20 nH) in package traces. If analog and digital circuits are fabricated on one chip, problems due to such inductances and the associated noise should be reduced.

Although the prototype converter was built for 16 bits, 15 bits was the maximum integral linearity achieved. This is the result of unexpectedly poor capacitor matching in the main DAC. To overcome this, the calibration range was increased by doubling the coupling capacitor between the main DAC and the calibration DAC at the cost of the

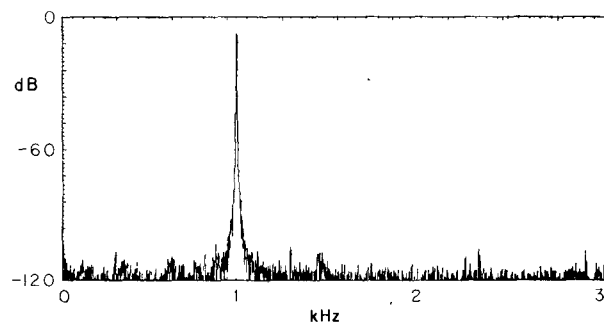


Fig. 9. Measured harmonic distortion of the converter obtained by computation of a 4096 point fast Fourier transform (FFT). Integral nonlinearity larger than about 1 LSB at 15 bits would show up as a noticeable spectral component at the second or third harmonic frequency.

TABLE II
PERFORMANCE CHARACTERISTICS OF CONVERTER MEASURED AT ROOM TEMPERATURE

Supply Voltages	± 5	V
Resolution	15	Bits
Linearity	15	Bits
Offset	$< \pm 1/4$	LSB
Conversion Time (for $\pm 1/2$ LSB Linearity)		
12 Bit	12	μs
15 Bit	80	μs
RMS Noise	40	μV
Power Dissipation (excludes logic)	20	mW
Die Area (excludes logic)	7.5	mm^2

calibration resolution. The calibration is now performed at a 17 bit level due to the increase in the coupling capacitor value, and 15 bits is the maximum linearity possible with this level of calibration resolution.

The plot of differential nonlinearity for all 32 768 codes is shown in Fig. 8. The data are obtained by a code density test [9]. In this test, the data were collected while the converter was running at a 12 kHz sampling rate with a 1 kHz sine wave input signal.

Integral nonlinearity was measured statically at the major carries. The maximum error observed was 1.6 LSB at 16 bits. For the interest of audio signal processing, fast Fourier transform was performed on the 4096 digital output codes obtained by sampling a 1 kHz input sine wave. As is shown in Fig. 9, no second or third harmonic distortion is observable.

The performance of the converter is summarized in Table II.

V. CONCLUSIONS

A self-calibrating A/D converter utilizing a capacitor array main DAC and a resistor string sub DAC is described. After the calibration, linearity of the converter was increased to 15 bits from 10 bit initial linearity. In addition to the closed loop offset cancellation, a simple digital offset correction technique is used to reduce the system offset to less than 60 μV . A folded cascode CMOS comparator

enables a fast high resolution conversion. A conversion rate of 12 kHz was achieved experimentally. A maximum conversion rate of 80 kHz was obtained at a 12 bit linearity level. The linearity at this speed should be improved by proper isolation of the analog circuits from the noisy digital circuits.

ACKNOWLEDGMENT

We gratefully acknowledge Dr. J. McCreary for helpful suggestions at the outset of this work, J. Doernberg for development of the test system, and Intel Corporation and Reticon Corporation for technical assistance. We appreciate helpful suggestions from reviewers.

REFERENCES

- [1] J. L. McCreary and P. R. Gray, "All MOS charge redistribution analog-to-digital conversion techniques—Part I," *IEEE J. Solid-State Circuits*, vol. SC-10, pp. 371–379, Dec. 1975.
- [2] A. R. Hamade, "A single chip all-MOS 8-bit A/D converter," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 785–791, Dec. 1978.
- [3] P. R. Gray, J. L. McCreary, and D. A. Hodges, "Weighted capacitor analog/digital converting apparatus and method," U.S. Patent 4129863, Oct. 1977.
- [4] D. A. Hodges, P. R. Gray, and J. L. McCreary, "Weighted capacitor analog digital converting apparatus and method," U.S. Patent 4200863, Dec. 1978.
- [5] H. S. Lee and D. A. Hodges, "Self-calibration technique for A/D converters," *IEEE Trans. Circuits Syst.*, vol. CAS-30, pp. 188–190, Mar. 1983.
- [6] B. Y. Kamath, R. G. Meyer, and P. R. Gray, "Relationship between frequency response and settling time of operational amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 347–352, Dec. 1974.
- [7] H. S. Lee and D. A. Hodges, "Accuracy consideration in self-calibrating A/D converters," submitted to *IEEE Trans. Circuits Syst.*
- [8] J. L. McCreary, "Matching properties, and voltage and temperature dependence of MOS capacitors," *IEEE J. Solid-State Circuits*, vol. SC-16, pp. 608–616, Dec. 1981.
- [9] J. Doernberg, H.-S. Lee, and D. A. Hodges, "Full-speed testing of A/D converters," *IEEE J. Solid-State Circuits*, this issue, pp. 820–827.



Hae-Seung Lee (S'84) was born in Seoul, Korea, on June 29, 1955. He received the B.S. and M.S. degrees from Seoul National University, Seoul, Korea, in 1978 and 1980, respectively, and the Ph.D. degree from University of California, Berkeley, in 1984.

In 1984 he joined the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA, where he is now an Assistant Professor.



David A. Hodges (S'59–M'65–SM'71–F'77) received the B.E.E. degree from Cornell University, Ithaca, NY, and the M.S. and Ph.D. in electrical engineering from the University of California, Berkeley.

From 1966 to 1970 he was with Bell Laboratories, first in the components area at Murray Hill, NJ, then as Head of the System Elements Research Department at Holmdel, NJ. Now is Professor of EECS at UC Berkeley, where he has been a member of the faculty since 1970. He is currently involved with colleagues and students in research on analog and digital integrated circuits, VLSI for telecommunications applications, and manufacturing information systems.

Dr. Hodges and his faculty colleagues, P. R. Gray and R. W. Brodersen, were co-recipients of the 1983 IEEE Morris Liebmann Award for work on switched-capacitor circuits. He is a member of the National Academy of Engineering.



Paul R. Gray (S'65–M'69–SM'76–F'81) was born in Jonesboro, AK, on December 8, 1942. He received the B.S., M.S., and Ph.D. degrees from the University of Arizona, Tucson, in 1963, 1965, and 1969, respectively.

In 1969 he joined the Research and Development Laboratory, Fairchild Semiconductor, Palo Alto, CA, where he was involved in the application of new technologies for analog integrated circuits, including power integrated circuits and data conversion circuits. In 1971 he joined the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, where he is now a Professor. His research interests during this period have included bipolar and MOS circuit design, electro-thermal interactions in integrated circuits, device modeling, telecommunications circuits, and analog/digital interfaces in VLSI systems.

Dr. Gray is the coauthor of a college textbook on analog integrated circuits. He has been corecipient of Best Paper Awards at the International Solid-State Circuits Conference and the European Solid-State Circuits Conference and was corecipient of the IEEE R. W. G. Baker Prize in 1980. He served as Editor of the *IEEE JOURNAL OF SOLID-STATE CIRCUITS* from 1977 through 1979, and as Program Chairman of the 1982 International Solid-State Circuits Conference.