### SA20.4: A ±2.45V-Swing CMOS Telescopic Operational Amplifier

K. Gulati, H-S. Lee

Massachusetts Institute of Technology, Cambridge, MA

A telescopic cascode opamp typically has a higher frequency capability and consumes less power than other topologies. The disadvantage of a telescopic opamp is severely limited output swing. In a conventional telescopic opamp shown in Figure 1, all transistors are biased in the saturation region. Transistors M1-M2, M7-M8 and the tail current source M9 must have at least  $V_{ds,sat}$  to offer a good common-mode rejection (CMRR). To allow for process and temperature variations, a small safety margin  $V_{margin}$  is often added to their  $V_{ds}$  to ensure saturation. The maximum differential output swing of a telescopic opamp is shown to be  $2V_{sup}$ - $10V_{ds,sat}$  of 200mV and  $V_{margin}$  of 100mV, the output swing is limited to  $2V_{sup}$ -2.6V. In a 3V supply system, this represents a 45% reduction of available output swing.

Although a telescopic opamp without the tail current source improves the differential swing by  $2V_{ds,sat}+2V_{margin}$  (600mV), the CMRR is compromised [1]. Moreover, performance parameters (such as unity-gain frequency) of an opamp with no tail or with a tail transistor in the linear region are sensitive to input common-mode and supply voltage variation which is undesirable in most analog systems.

This telescopic opamp offers higher output swing than a conventional telescopic amplifier while maintaining high CMRR and supply rejection (PSRR), and ensuring constant performance parameters (Figure 2) . Transistors M7-M8, and M9 are deliberately driven deep into the linear region. Since they normally operate in the linear region,  $V_{margin}$  is not needed. The output swing is improved by 0.7V from a telescopic amplifier and becomes comparable to a folded cascode amplifier. The reduction of gain and CMRR due to the low output resistance in the linear region is compensated by gain enhancement and replica tail feedback, respectively. The gain enhancement employs the well-known differential regulated cascode structure except the control voltage  $V_{ncontrol}$  is chosen to bias M7-M8 in the linear region [2]. The gain enhancement amplifier A2' incorporates the replica tail feedback to keep the drain current of M9 constant despite input common-mode voltage variation.

The basic goal of the replica tail feedback is to keep the tail current constant (Figure 3). It accomplishes this by modulating the gate voltage of the tail transistor. Transistors M1, M2 and M9 represent the input devices and tail current source of a differential amplifier, while M1R, M2R and M9R form their corresponding replicas. Amplifier A<sub>a</sub> is in negative feedback across the replica circuitry which forces the voltage at node y to equal the voltage at pcontrol. Also, A2' forces the commonmode component of the drain voltages of M1 and M2 to equal the voltage at *pcontrol*. Under these conditions, the voltage at the drain of the tail transistor (node *a*) always equals the voltage at the drain of the replica tail transistor (node *b*). Since current through M9R is fixed by I<sub>c</sub>, current through M9 remains fixed even if it is biased in the deep linear region. A similar technique was proposed for the tail current of a 2-stage amplifier, with no silicon results [3]. This method provides superior CMRR and PSRR by ensuring proper replica-main circuit match by making use of a gain-enhancement amplifier.

When the main and replica circuits are perfectly matched, small-signal analysis shows that the effective output resistance of the tail-current transistor can be approximated as:

 $Rtail = ro_{g} \cdot Ao \cdot (gm_{gR} \cdot ro_{gR}) \cdot (gm_{1R} \cdot ro_{1R})$ 

Since M9R is in the linear region,  $gm_{gR} \cdot ro_{gR}$  is less than unity. Thus, the enhancement is primarily provided by  $Ao \cdot (gm_{gR} \cdot ro_{gR})$ . The 3dB frequency for the CMRR is located at the pole of the open-loop transfer function of the replica tail feedback loop. Mismatch between the main and replica circuits reduces CMRR at dc and shifts the 3dB location to higher frequencies.

To minimize power consumption and area, transistor widths and current in the replica circuitry are scaled down by a factor of 4 with respect to the main opamp. Capacitance C3 is the polesplitting frequency compensation for the common-mode loop, as shown by the dashed path in Figure 2.

The internal structures of amplifiers A1 and A2' are depicted in Figures 4a and 4b, respectively. A1 is a conventional foldedcascode amplifier. The third input (applied at the gate of transistor M5E) sets the common-mode drain voltages of M7 and M8 in the main amplifier.Amplifier A2' is similar except for the third input transistor which is split to create an amplifier (consisting of transistors M3X, M4X, M7X and M8X in the shaded region) to serve as Ao for the replica tail as shown in Figure 3. No extra power is required to construct this amplifier as it replaces the third transistor. Since the differential gainenhancement amplifier (with input transistors M1X and M2X) is in common-mode unity gain feedback across the cascode devices in the telescopic amplifier, the common-mode voltage at the inputs of this enhancement amplifier equals the commonmode voltage of the inputs of amplifier A. Furthermore, since amplifier A<sub>a</sub> is in negative feedback, its inputs are virtually shorted. Hence the voltage at the drain of transistors M1R and M2R (node y), as shown in Figure 3, tracks the common-mode voltage at the drains of transistors M1 and M2, ensuring good main-replica matching. The power consumed by amplifiers A1 and A2' combined is about a third of the total power consumption of the opamp.

The opamp is implemented in  $0.8\mu$ m CMOS and occupies a  $600x630\mu$ m<sup>2</sup> die. Figure 5a shows the transfer characteristic of the amplifier. The hysteresis-type behavior is due to the 500Hz input frequency. Figure 5b shows the large signal step response of the amplifier. The 1% settling time is measured to be 26ns. The slight discrepancy from simulations is attributed to the settling time of the input waveform itself. The chip specifications and performance summary are given in Tables 1 and 2, respectively. The chip micrograph is shown in Figure 6.

#### Acknowledgments:

This research was funded by DARPA under agreement DAAL-01-95-K-3526. The authors thank J. Lloyd, S. Narendra, M. Varghese, A. Shabra, P. Naik and D. Martin for their help.

#### References:

[1] Nicollini, G., et al., "High Frequency Fully Differential Filter Using Operational Amplifiers Without Common-mode Feedback," IEEE J. of Solid-State Circuits, vol. 24, no. 3, June, 1989.

[2] Yang, J., H.-S. Lee, "A CMOS 12-bit 4MHz Pipelined A/D Converter with Commutative Feedback Capacitor," CICC 1996.

[3] Krenik, W., et al., "High Dynamic Range CMOS Amplifier Design in Reduced Supply Voltage Environment," Tech. Dig. Midwest Sym. on Circuits and Systems, 1988.



Figure 1: Conventional telescopic amplifier.



Figure 2: Implementation of operational amplifier.



Figure 3: Basic concept of replica tail feedback.









Figure 5: Opamp measurements (a) transfer function; (b) large-signal step response (horz: 20ns/div, vert: 200mV/div considering picoprobe attenuation).

Technology	0.8µm CMOS
Power Supply	3.3 V
Die Size	600µm x 630µm
Power Consumption	4.8 mW

### Table 1: Chip specifications.

	Simulation	Measurement
Differential Open Loop Gain (500Hz)	105dB	90 dB
Differential Output Swing	+/- 2.4V	+/- 2.45V
Unity Gain Frequency (Output Load=3.52pf)	93MHz	90MHz
Phase Margin	78degs	
Settling Time (1%; noise gain > 2, Output Load ~ 3.65pF)	17.3ns	26ns
Slew Rate	133mv/ns	125mv/ns
Offset (typical)	9.5mv	1-2mv
CMRR (500Hz)	57dB	>50dB

## Table 2:Opamp measured and simulated<br/>performance.





Figure 6: Chip micrograph.





Figure 1: Conventional telescopic amplifier.



Figure 2: Implementation of operational amplifier.





Figure 3: Basic concept of replica tail feedback.





Figure 4: Gain enhancement amplifiers, a: left, b: right.





Figure 5: Opamp measurements (a) transfer function; (b) large-signal step response (horz: 20ns/div, vert: 200mV/div considering picoprobe attenuation).









# Technology Power Supply Die Size Power Consumption

0.8μm CMOS 3.3 V 600μm x 630μm 4.8 mW

Table 1:Chip specifications.



	Simulation	Measurement
Differential Open Loop Gain (500Hz)	105dB	90 dB
Differential Output Swing	+/- 2.4V	+/- 2.45V
Unity Gain Frequency (Output Load=3.52pf)	93MHz	90MHz
Phase Margin	78degs	
Settling Time (1%; noise gain > 2, Output Load ~ 3.65pF)	17.3ns	26ns
Slew Rate	133mv/ns	125mv/ns
Offset (typical)	9.5mv	1-2mv
CMRR (500Hz)	57dB	>50dB

# Table 2:Opamp measured and simulated<br/>performance.

