A 12-bit Mismatch-Shaped Pipeline A/D Converter

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Abstract

This paper presents pipeline A/D converters with improved linearity. The linearity improvement is achieved through a combination of oversampling and mismatch shaping, which modulates the distortion energy out-of-band. A 77dB SFDR is achieved at an oversampling ratio of 4 and a sampling rate of 51Msample/s, which is a 12dB improvement compared to a converter with no mismatch shaping. These results were obtained from a test chip fabricated in a 0.35μm CMOS process.

Introduction

In recent years, delta-sigma modulators and pipeline converters have been considered as possible realizations of analog-to-digital converters for wide-band signals. In comparing these converters, we recognize a few important attributes. Due to the wide bandwidth of the input signal and limited circuit speed, delta-sigma converters afford only low oversampling ratios, which makes high-resolution conversion extremely difficult. The low oversampling ratio generally nullifies the primary advantage of delta-sigma converters; the tolerance to component mismatches. In this regard, remaining potential advantages of delta-sigma converters over pipeline converters now only include ease of anti-alias filtering and low quantization noise. It must be noted that the ease of anti-aliasing is not inherent to delta-sigma modulation. Rather, it is associated with oversampling. Therefore, pipeline converters can experience the same benefit of easy anti-aliasing by simply operating the converter at higher sampling rate than the Nyquist rate, i.e., oversampling. As for quantization noise in pipeline converters, the quantization noise can be made smaller by adding more stages at the end of the pipeline. Since the last stages of the pipeline do not contribute much thermal noise, they can be made extremely small and low power. Therefore, the quantization noise itself can be made arbitrarily small with negligible increase of area and power. Certainly, doing so will not improve the accuracy or thermal noise. However, it is no different in delta-sigma converters with low oversampling ratio.

Based on the above observation, we can conclude that delta-sigma converters do not possess any fundamental advantage over pipeline converters for wide-band applications that necessitate low oversampling ratios. At this low oversampling ratio many delta-sigma converters are incapable of providing good enough performance. While there are a few examples of delta sigma convertets with a low oversampling ratio[1,2], we believe that a more efficient approach would be to oversample a standard pipeline converter, and shape the distortion due to mismatch out of the signal band, where it will be removed by a subsequent digital filter. Since no attempt is made to shape the quantization noise, there are none of the concerns associated with delta-sigma converters with a low oversampling ratio. The theory of oversampled pipeline converters has been reported earlier[3], here we discuss the design and experimental results from a 0.35μm CMOS prototype.

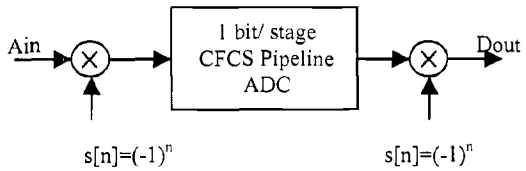

Fig. 1 Block diagram of mismatch shaping converter.

Mismatch Shaping in Pipeline ADC

A pipeline converter that exploits the mismatch shaping idea is shown in fig. 1. It has at its core a 1 bit per sage implementation of the commutative feedback capacitor scheme (CFCS) pipeline converter proposed in [4]. The 1 bit per stage CFCS converter has an even integral nonlinearity (INL) in presence of capacitor mismatch. An example transfer characteristic, which assumes a Δ capacitor mismatch only in the first stage of the pipeline, is shown in fig. 2(a).

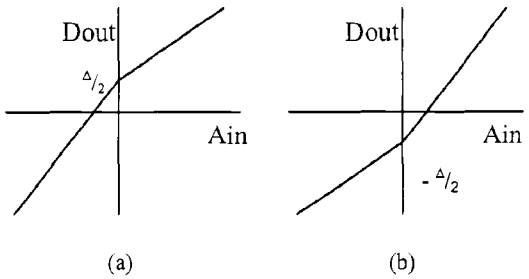

Fig. 2 Converter transfer characteristics (a) s = 1 (b) s = −1

If the input to the CFCS is multiplied by -1 at alternating sampling phases, and its digital output is also multiplied by -1 during those phases as shown in fig. 1, then the converter characteristics simply alternates between the characteristics in fig. 2 (a) and (b), at a rate equal to the sampling frequency. We see that the average converter characteristic will be very close to the ideal one and the error is modulated to half the sampling rate.

If the analog input is DC, the error is indeed modulated to half the sampling frequency where can be removed by a digital low pass filter. If the input has a finite bandwith, then the spectrum of the distortion of the mismatch shaped converter in fig. 1 is the same as the distortion spectrum that would be introduce by the core CFCS converter alone, except that the distortion is modulated to half that sampling frequency. This results in the strong lower order distortion components being moved out of band. Although some of the weak higher order distortion components may alias back into the signal band, this technique significantly improve the linearity of the converter even at oversampling ratios as low as 4.

It should be noted that a core with even INL is essential for this scheme to work. If a core with odd INL were to be used, then the input will pass through the same characteristic during all sampling phases and the distortion will not be shaped to higher frequencies.

In a fully differential implementation multiplying the input with -1 can be realized by swapping the polarity of the input applied to the CFCS stage, an operation that has a very simple circuit realization. The multiplication in the digital domain can also be realized very simply. Moreover, the implementation of the 1 bit per stage CFCS pipeline converter only requires a very slight modification of the standard pipeline stage comparator logic, to give the even INL, which is accomplished by making the capacitor that is connected in feedback around the stage amplifier dependent on the decision bit of the stage[4]. It can be concluded, therefore, that the circuit implementation of this idea only entail little added complexity. Although a digital low-pass filter is need to removed the out-of-band distortion, this filter would serve the dual purpose of augmenting the function of the weak analog anti-aliasing filter.

On the Use of Noise Shaped Sequences

In fig.1 the sequence s[n] is a deterministic alternating sequence and is used to modulated the distortion energy to half the sampling frequency. It is possible to whiten the distortion tones that fold back into the signal band through the use of a noise shaped sequence. Since the spectrum of the distortion gets convolved with the spectrum of the sequence s[n], it is desirable that s[n] have most of its energy concentrated in a narrow band around half the sampling frequency as shown in fig. 3. The wider the spectrum of s[n], the large the energy that will leak back into the signal band, and in the limit of using a white sequence for s[n], the distortion spectrum gets whitened. This is clearly not the optimal from a signal to noise ratio stand point, when compared to the use of a narrow band signal for s[n].

Impact of Circuit Non-idealities

The techniques presented in this paper hinge on the even nature of the INL characteristics of the 1 bit per stage CFCS converter, which results in presence of capacitor mismatch. Practically, the INL will also contain odd terms due to effects such as finite opamp gain and input dependent charge injection. The distortion introduced due to these effects will not be pushed out-of-band through mismatch shaping and will impact the linearity of the converter. Fortunately, the impact of these non-idealities can be minimized through careful circuit design to the extent that is required by the application at hand.

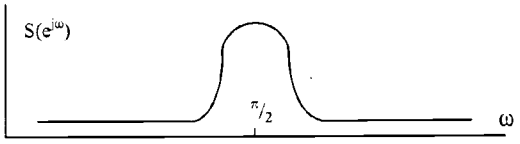

Fig. 3 Spectrum of a noise shaped sequence s[n]

Test Chip Architecture

Fig. 4 shows the architecture of the ADC. Each of the pipeline stages implements the CFCS concept. Stage 2 through 11 have a residue diagram shown in fig. 5. The manner in which the over-range correction is implemented results in a 3 bits output for each of these stages. The pipeline stages are scaled from stage 2 through 4 by a factor of 2 per stage to minimize the power consumption. Although the target resolution of the converter is 12 bits, it produces a 15 bits output to make the converter noise floor dominated by thermal noise. The quantization noise floor is reduced by the 4-bit flash is used at the back-end of the converter.

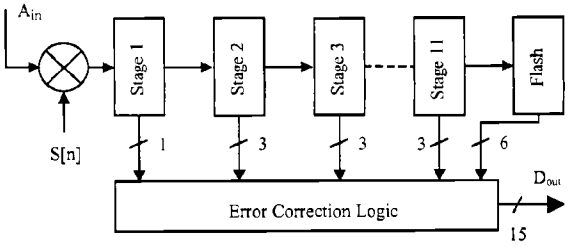

Fig. 4 Test chip architecture

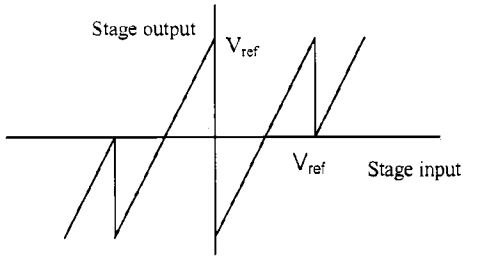

Fig. 5 Residue diagram of stage 2 through 11

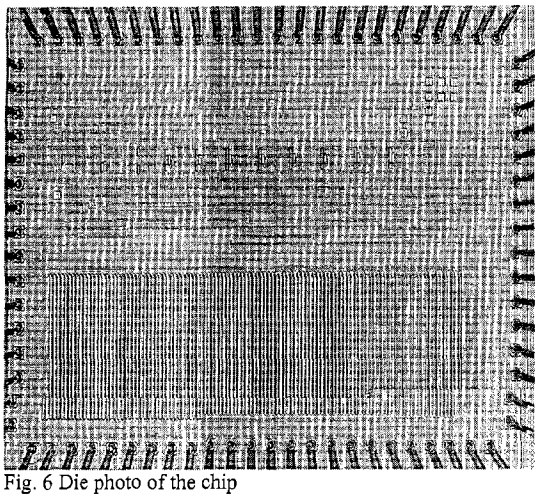

Fig. 6 Die photo of the chip

The test chip was designed in a 0.35μm CMOS process with poly to poly capacitors. A die photo of the chip is shown in fig. 6.

Experimental Results

Fig. 7 and 8 respectively show the spectrum of the output of the ADC without and with mismatch shaping as implemented in fig. 1. As expected the distortion gets modulated to half the sampling frequency when mismatch shaping is applied. The dominant distortion components fall out of band, resulting in a 12 db improvement is SFDR, an 11dB improvement in THD and a 5dB improvement in SNDR at an oversampling ratio of 4. The SNDR figure is dominated by thermal noise. These results are obtained at a sampling frequency of 51Msample/s and an input of 475KHz. Fig 9 and 10 show the INL of the converter without and with mismatch shaping respectively. Fig. 11 and 12 show the DNL without and with mismatch shaping. The INL and DNL plots are obtained from the measured data after it has been filter digitally to remove the out-of-band signals. Fig. 13 plots the SNDR and SFDR as a function of the clock frequency.

Table 1 summarizes the measured performance of the ADC.

Acknowledgments

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References

[1] T. L. Brooks, D. W. Robertson, D. F. Kelly, A .Del Muro, and S. W. Harston, "A 16b SD Pipeline ADC with 2.5 MHz output Data-Rate," Digest of Technical Papers, 1997 ISSCC, pp. 208-209, San Francisco, Feb. 1997.

[2] E. T. King, A. Eshraghi, I. Galton and T. Fiez, "A Nyquist-Rate Delta-Sigma A/D Converter," IEEEJournal of Solid-State Circuits, vol. 33, no. 1, January, 1998.

[3] A. Shabra, H.-S. Lee. L. Hernandez, "Oversampled pipeline A/D Converters with Mismatch Shaping," Electronic Letters, vol. 34, no. 6, 19 March 1998, p508-9.

[4] P. C Yu. and H.-S. Lee, "A Pipeline A/D Conversion Technique with Near-Inherent Monotonicity," IEEE Trans. Circuits & Systems, vol. 42, pp. 500-501, July, 1995.

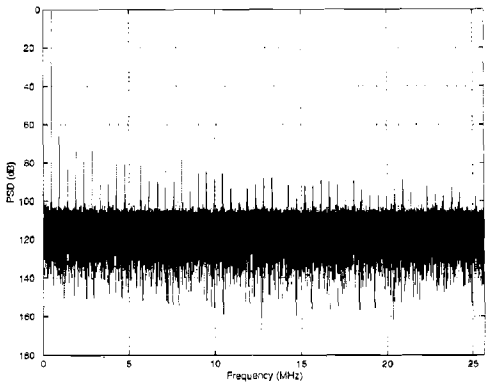

Fig. 7 ADC output spectrum without mismatch shaping (fs=51.3337MHz fin=0.475MHz)

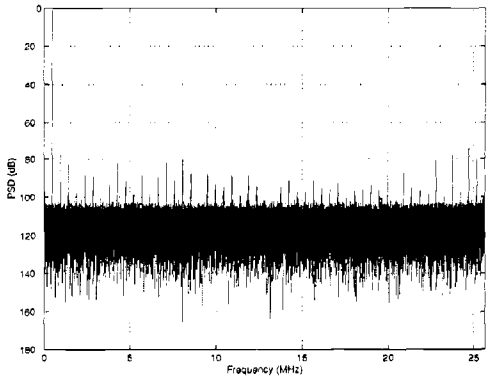

Fig. 8 ADC output spectrum with mismatch shaping applied (fs=51.3337MHz fin=0.475MHz)

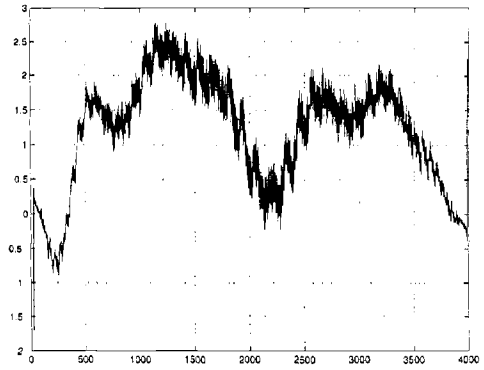

Fig. 9 INL without mismatch shaping for filtered data (fs=51.3337MHz)

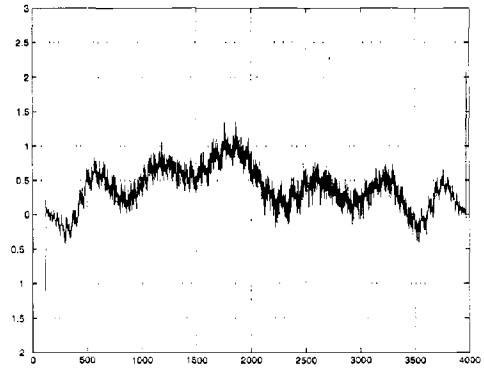

Fig. INL with mismatch shaping for filtered data (fs=51.3337MHz)

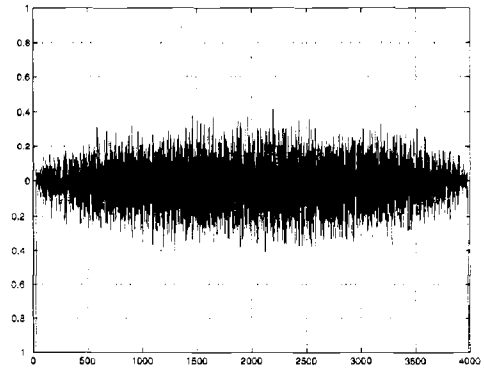

Fig. 11 DNL without mismatch shaping for filtered data (fs=51.3337MHz)

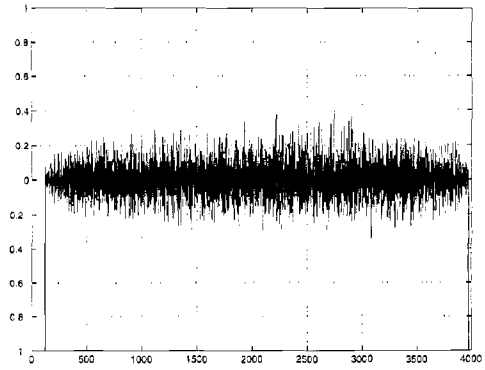

Fig. 12 ADC DNL with mismatch shaping for filtered data (fs=51.3337MHz)

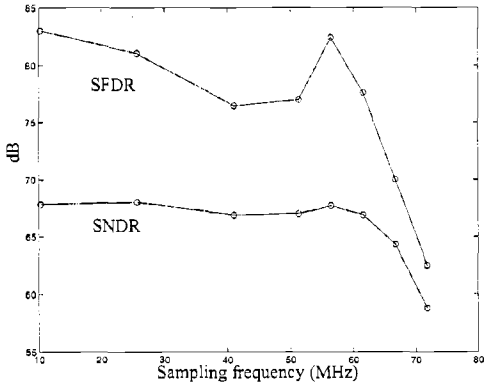

Fig. 13 SNDR and SFDR vs sampling frequency (fin = 0.475MHz)

TABLE 1
Summary of the measured performance

Process	0.35um CMOS
Resolution	12bits
Supply Voltage	3.4V
Differential Input Range	1.4Vpp
Sampling Rate	51Msample/s
SNDR (w/o MS)	62dB
SNDR (with MS)	67dB
SFDR (w/o MS)	65dB
SFDR (with MS)	77dB
THD (w/o MS)	64dB
THD (with MS)	75dB
Analog Power Dissipation	435 mW
Digital Power Dissipation	165 mW