SESSION 14: ANALOG PROCESSORS

THPM 14.1: A 200MHz CMOS Phase-Locked Loop with Dual Phase Oetectors*

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DATA COMMUNICATIONS applications are pushing phase-locked loop (PLL) frequencies ever higher[1,2]. This paper describes a 200MHz PLL in a 2-micron CMOS technology. In conventional PLLs, a high-frequency variable oscillator is usually made with either a frequency multiplier and crystal reference, or a trimmed external resonant circuit. The former has a narrow tuning range, while the latter is expensive. In this paper, we have employed an untrimmed current-controlled ring oscillator (CCO). Part-to-part variation of the free-running frequency and small loop bandwidth, necessary to minimize data-dependent jitter, can cause a PLL with only a mixer phase detector to fail to acquire the data frequency[3]. On the other hand, a PLL with only a frequency detector will acquire the wrong frequency due to missing pulses at the input. In this circuit, to overcome these problems, two phase detectors are included – a phase-frequency detector (PFD) for fast acquisition during data preamble (100% pulse density), and a mixer phase detector to lock on actual data (in the presence of missing pulses).

The system includes an external RC loop filter (Figure 1). Paths for the variable oscillator and external frequency signals are symmetric. The voltage-to-current converter (V-I) has a differential input and single-ended output. The blocks labeled PS are phase splitters. Each divide-by-four block contains two D flip-flops which accomodate the lower operating frequency of the PFD. Low-impedance outputs for frequencies f_{LO} and f_{XO} are capable of driving a 50Ω line. Internal 200MHz clock signals are not brought out to the pins. A three-amplifier ring is used in the CCO (Figure 2). Each amplifier has an inverter in parallel with a current-limited inverter. The output is buffered and level-shifted by two inverters. The oscillator voltage-to-frequency conversion factor is 16MHz/V. The sensitivity of the center frequency, f_C, with respect to $(V_{DD} - V_{RR})$ is 20%/V. A feedback circuit forces V_{RR} to track V_{REF} which in turn tracks V_{DD}, reducing the sensitivity of f_C to V_{DD}. Also, the f_C temperature coefficient is cancelled by introducing temperature dependence in V_{REF}.

The bandgap reference provides temperature- and supply-independent bias to the voltage-to-current converter, as well as generating V_{REF} (Figure 3). The circuit is an extension of a simple bandgap reference[4]. A temperature-dependent current through R6 induces a voltage that is proportional to absolute temperature. This voltage, together with an NPN transistor, creates V_{REF}, whose temperature dependence cancels that of the CCO. Figure 4 shows the mixer phase detector comprising four cross-coupled tri-state inverters. The output is a differential current. With symmetric phase splitter drive, the differential output offset current is small.

The PFD consists of four S-R flip-flops, a NOR gate, and a differential charge-pump output circuit. The output can be disabled by MOS switches when frequency acquisition is completed. Depending on the application, disabling of the PFD can be done by a circuit that detects the end of frequency acquisition.

Figure 5 is a micrograph of the active portion of an IC fabricated with the $2\mu m$ scalable CMOS P-well process[5]. Without the bandgap reference, the circuit displays supply and temperature sensitivities which are large: 20%/V and -2200ppm/°C, respectively. Experimental results for typical circuits are stated in Table 1. The part-to-part variation figure is based on measurements of 15 prototype circuits from a single lot.

Simulations and experimental data using an external current source suggest that using the bandgap reference, the CCO supply sensitivity will be 4%/V and the CCO temperature coefficient will be about 500ppm/°C. The CCO is being modified to increase its range to ±25%.

Internal input and output waveforms in lock were measured from buffered test pads with a low-capacitance wideband buffered probe (Figure 6). Two on-chip inverters in series are used to amplify the 0.5Vrms sine wave input signal, generating a square wave for the PLL input. Spectra near the fundamental frequency of the input and output waveforms coincide down to the noise floor of the measurement equipment because of the large open-loop gain of the system (Figure 7).

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[1] Leonowich, R.H. and Steininger, J.M., "A 45MHz CMOS Phase/Frequency-Locked Loop Timing Recovery Circuit", *ISSCC DIGEST OF TECHNICALS PAPERS*, p. 14-15; Feb., 1988.

[2] Kato, K. et al, "A Low-Power 128MHz VCO for Monolithic PLL ICs", *IEEE Journal of Solid-State Circuits*, Vol. 23, p. 474-479; Apr., 1988.

[3] Gardner, F.M., *Phase-Lock Techniques*, 2nd Ed. John Wiley & Sons, Section 5.3, New York: 1979.

[4] Gray, P.R. and Meyer, R.G., *Analysis and Design of Analog Integrated Circuits*, 2nd Ed., p. 736-737, John Wiley & Sons, New York: 1984.

[5] Tomovich, C., "MOSIS — A Gateway to Silicon", *IEEE Circuits and Devices Mag.*, Vol. 4, p. 22-23; Mar., 1988.

Center Frequency	$200MHz$
Frequency Range	±17%
Part-to-part Center Frequency Variation, worst case in one process run	±8%
Active Die Area	$1.5mm \times 3.7mm$
Supply Voltage	$5V$
Power Consumption	$500\ mW$

TABLE 1—Experimental results.

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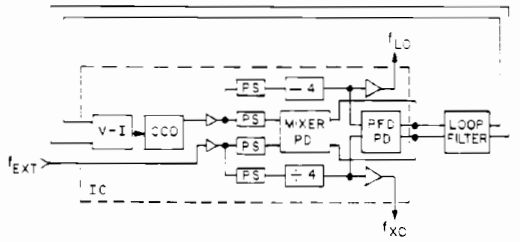

FIGURE 1–PLL block diagram.

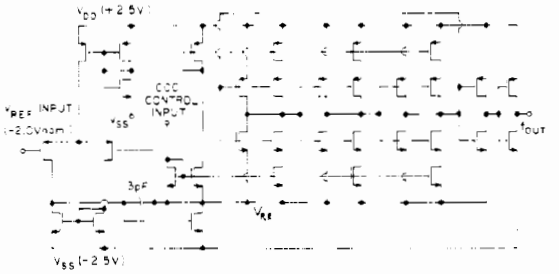

FIGURE 2–Current-controlled oscillator schematic diagram.

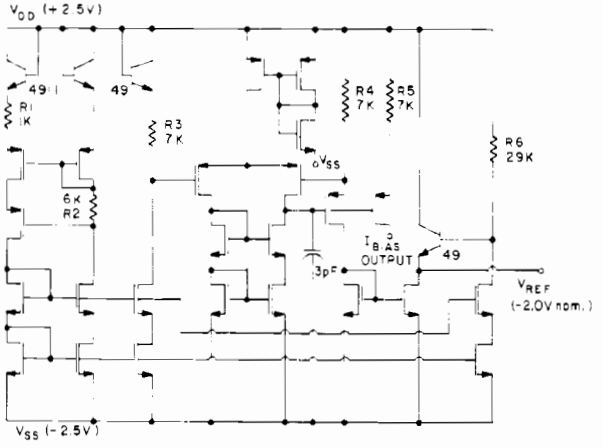

FIGURE 3–Bandgap reference schematic diagram.

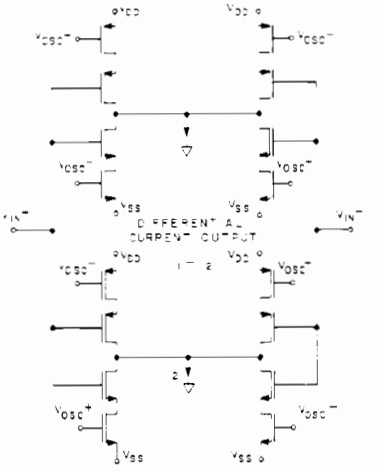

FIGURE 4–Mixer phase detector schematic diagram.

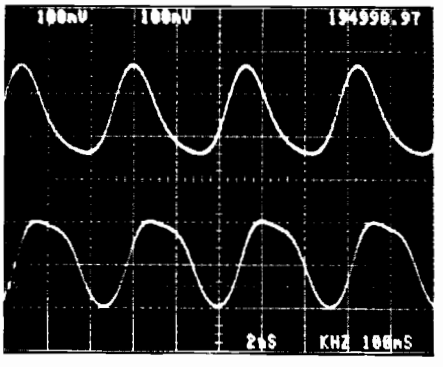

FIGURE 6–PLL internal waveforms in locked condition; top is buffered input, bottom is buffered CCO output. Vertical scale: 2V/div. Horizontal scale: 2ns/div.

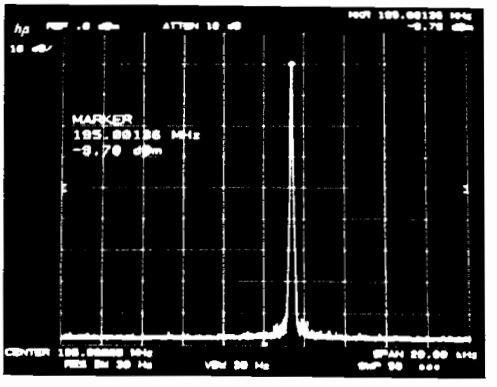

FIGURE 7–Coinciding spectra of PLL internal input and output waveforms, in locked condition. Vertical scale: 1-dBm/div, the top line corresponds to +26dBm. Horizontal scale: 2kHz/div. Center frequency: 195MHz.

FIGURE 5 – *See page 338*

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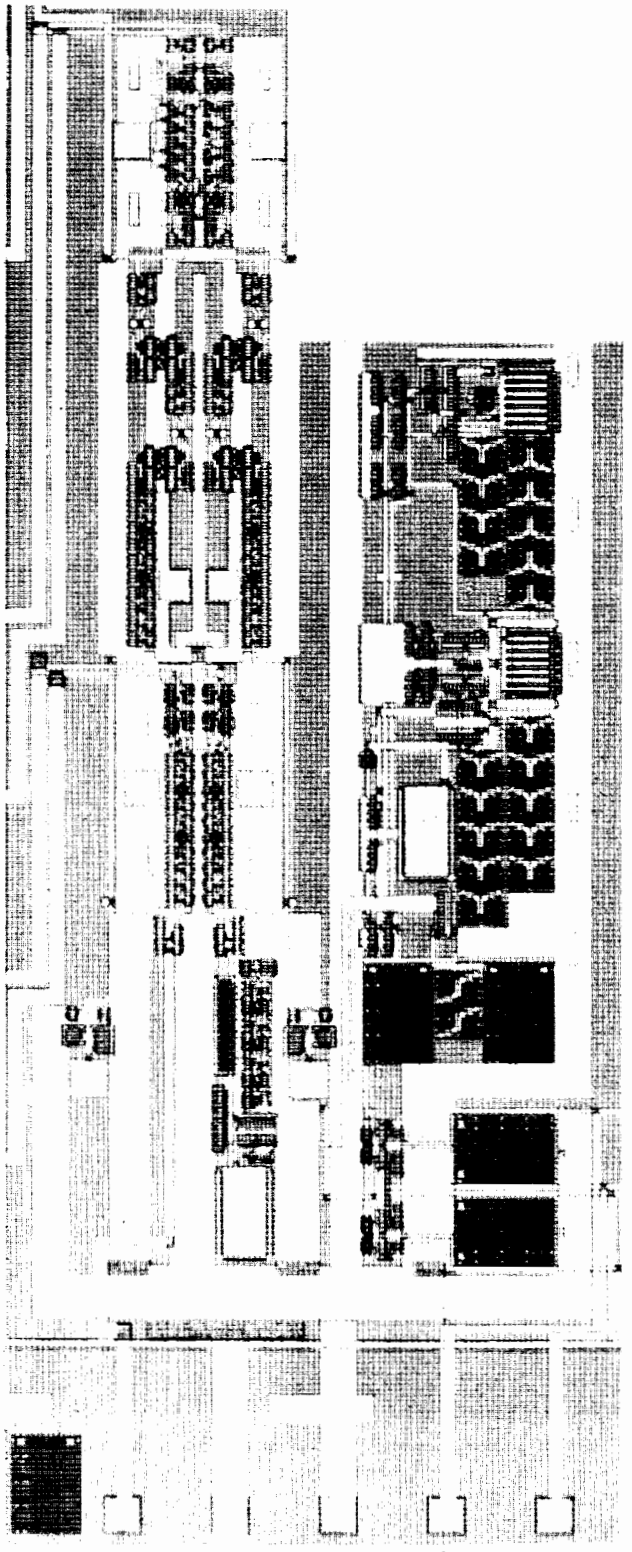

FIGURE 5–PLL die micrograph.