SESSION 10: Analog-to-Digital Converters

TPM 10.6: An 18b 10μs Self-Calibrating ADC

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AUTO-CALIBRATION has been used in monolithic ADCs to extend the limits of accuracy and stability imposed by processing, packaging, temperature, and aging[1,2]. This paper describes a self-calibrating, 18-bit, serial-output, 100ksps ADC which is implemented on two chips: a 24V BiCMOS analog chip, and a 5V 2μm CMOS digital chip. This partitioning allows a larger input signal for better dynamic range, eases the comparator design, and protects analog circuitry from digital feedthrough.

A block diagram of the circuit is shown in Figure 1. The two chips are shown as wired in a 7.6mm-wide, 16-pin plastic DIP. Thirteen inter-chip bonds make up the control and data interface. The only other common connections to the logic supply and its ground return are made through separate wires for each chip.

The analog chip is a charge-balancing converter: it comprises an 18-bit calibrated DAC, an auto-zeroed latching comparator, buffers for all analog inputs and logic for the self-timed interface to the digital chip.

The digital chip is a custom micro-controller which implements the calibration and conversion algorithms as well as the digital part of the user interface. The data path on this chip includes calibration pattern generators, a successive approximation register (SAR), elements to calculate the error terms and RAM to store those terms. This design uses all these components, except the pattern generator, for both calibration and conversion functions.

The circuit uses a successive approximation routine to arrive at the 18-bit result. Figure 2 shows the three components of the DAC with which the algorithm operates. The top 9 bits are implemented with a capacitor array. The next 7 bits are derived with a polysilicon resistor-string sub DAC, which interpolates the voltage on an extra unit capacitor in the main array. The last 2 bits of each 18-bit result are obtained by using the bottom two bits of the calDAC, a second resistor-string DAC whose primary function is correcting the errors in the main array.

During calibration, the calDAC is controlled by the SAR to quantify the differences between each capacitor and the sum of all smaller capacitors in the main array. Correction values for each capacitor are calculated using these differences and then stored in RAM. Whenever a bit is used during conversion, its correction value is applied through the calDAC.

In order to avoid the accumulation of digital truncation errors, storage and manipulation of the correction values are done at extended resolution, The effect of noise during calibration is reduced by averaging multiple error measurements.

During each SAR cycle three transfers of data must occur between chips after the comparator has settled. First, the comparator data must be latched and then read by the digital chip. Second, the next SAR output must be placed on the bus and then read by the analog chip. Third, the correction data must be placed on the bus for the calDAC. Figure 3 shows the inter-chip timing. Each of the time intervals (t_1, t_2, t_3) associated with these data transfers are made to track the gate delays of the appropriate chip, so that the time for comparator settling is maximized.

The analog circuitry is shown in more detail in Figure 4. This topology is fully differential for power supply rejection. Both the input signal and its ground reference are sampled by using two capacitor arrays, with the sampling switches returned to common. The comparator is auto-zeroed by storing the offset of each stage at its output. Open-loop auto-zeroing in this way allows noise and bandwidth to be optimized independently. Common-mode feedback is not required because the gain of each stage is low.

NPN diodes have been employed in the first stage (Figure 5) to eliminate MOS threshold voltage hysteresis due to overdrive[3]. The effect of hysteresis occurring in later stages is reduced by the gain to that point.

The FFT of Figure 6 was obtained for a 0dB, 1kHz input sampled at 96kHz. The total harmonic distortion was measured at −100dB. Micrographs of the 3.3x5.4mm analog chip and the 3.3x3.4mm digital chip are shown in Figure 7 and Figure 8, respectively.

Acknowledgment

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[1] Lee, H-S., et al., "A Self-Calibrating 15b CMOS A/D Converter", IEEE J. Solid-State Circuits, Vol. SC-19, p813-819; Dec., 1984.

[2] Croteau, J., et al., "Autocalibration Cements 16-bit Performance", Electronic Design, Vol. 34, No. 20, p101-106;; Sept., 1986.

[3] Tewksbury, T.L., et al., "The Effects of Oxide Traps on the Large-Signal Transient Response of Analog MOS Circuits", IEEE J. Solid-State Circuits, Vol. 24, p542-544, April, 1989.

Input voltage range	20Vp-p
Input signal bandwidth	dc to 500Hz
Dynamic range	123dB
Signal-to-distortion ratio	126dB
Clock frequency	1.024MHz
Sampling rate	256kHz
Output word rate	32kHz
Power supply voltages	+5.0V, −5.0V, GND
Power dissipation	120mW
Chip dimensions	4.48x6.53mm
Package type	28-pin PLCC/LCC

TABLE 1—Chip performance.

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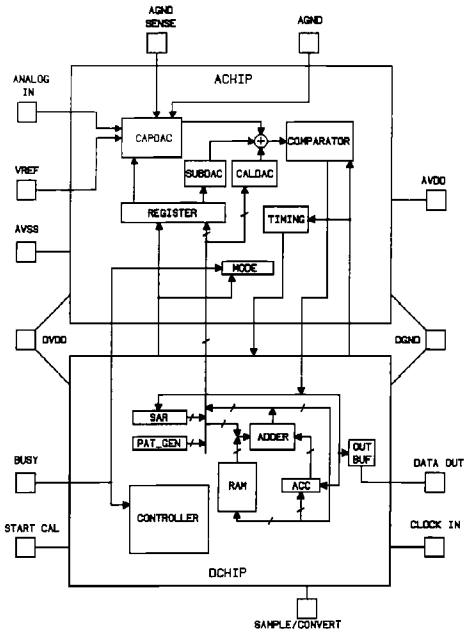

FIGURE 1—Block diagram of 18b ADC.

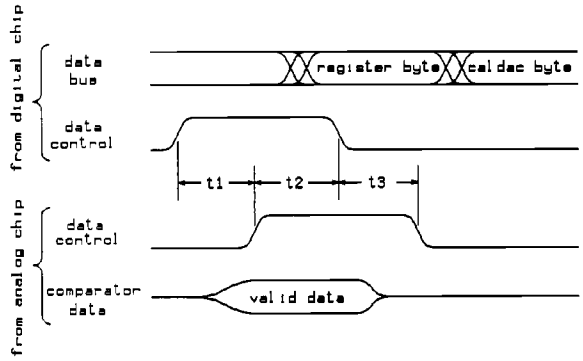

FIGURE 3—Inter-chip timing.

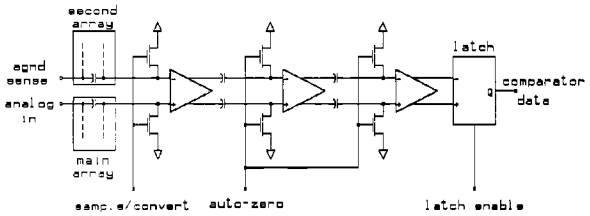

FIGURE 4—Simplified analog circuitry.

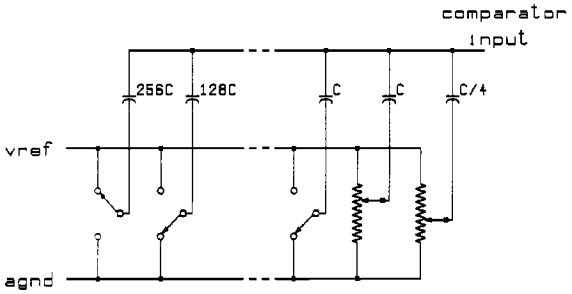

FIGURE 2—Simplified 18b DAC.

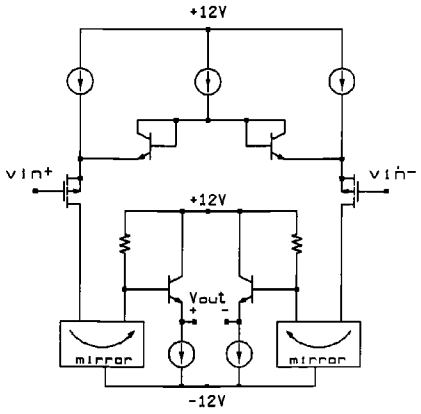

FIGURE 5—Simplified first stage of comparator.

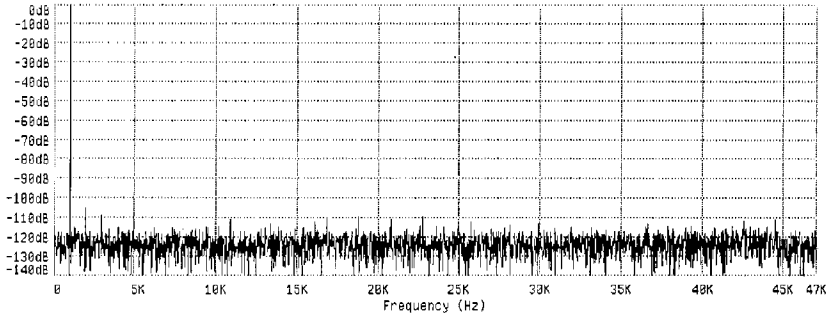

FIGURE 6—Measured results.

FIGURES 7, 8, 9 — *See page 292*

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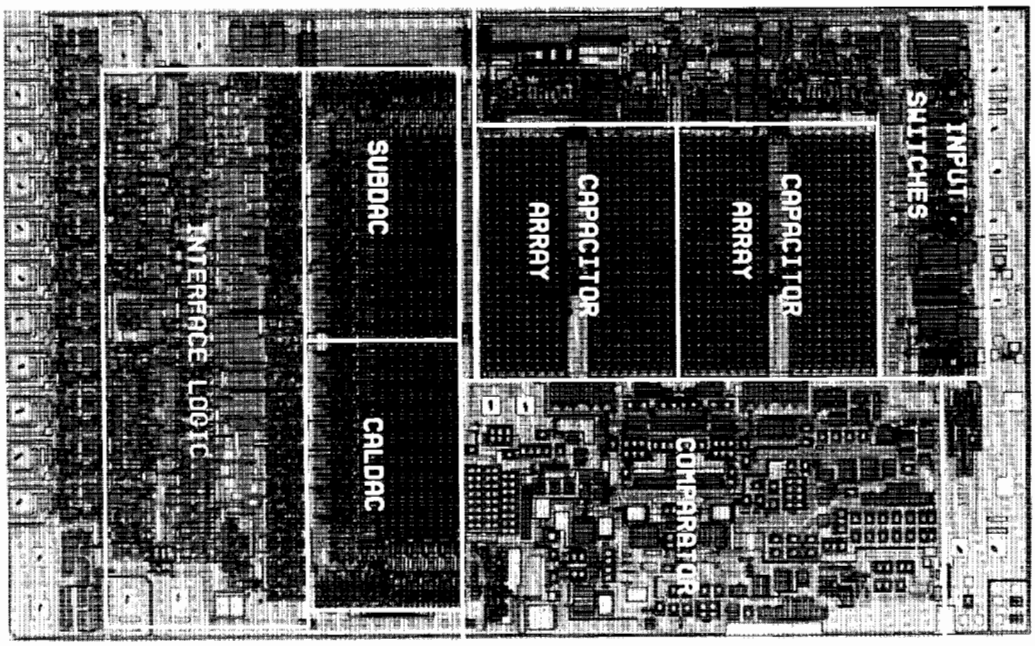

FIGURE 7—Analog chip micrograph.

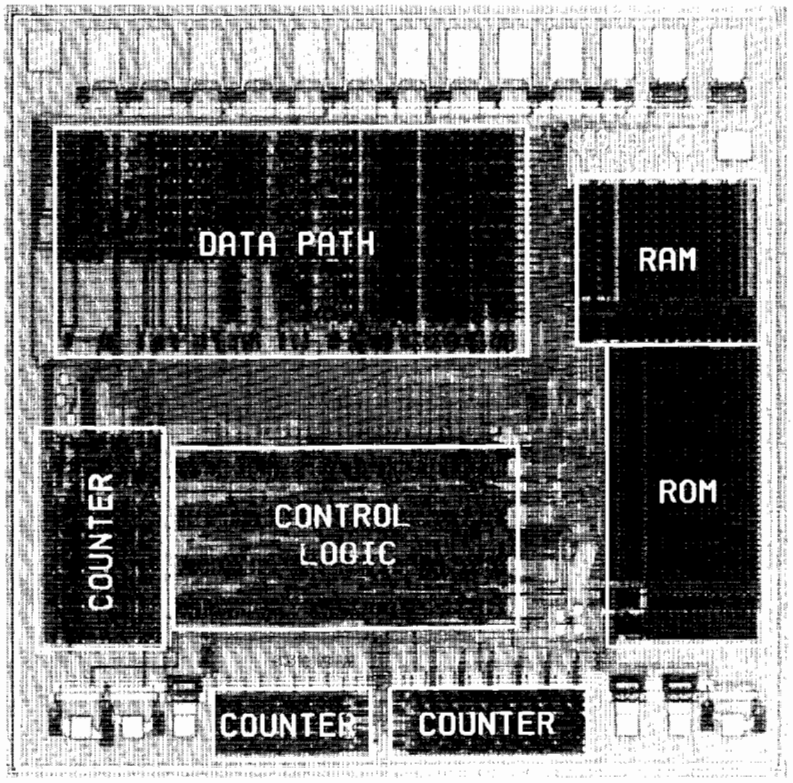

FIGURE 8—Digital chip micrograph.

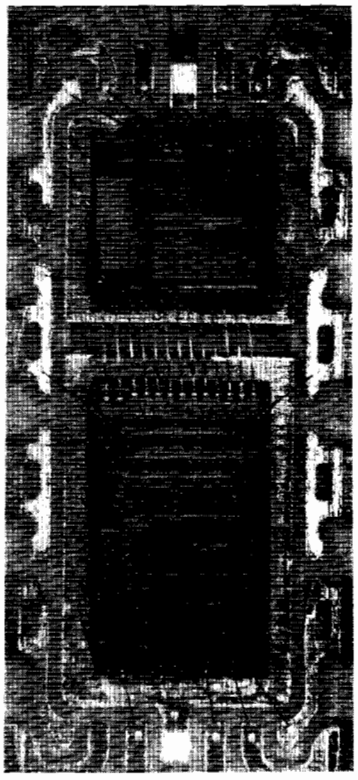

FIGURE 9—Assembled leadframe prior to plastic encasement.