A 12 BIT 600kS/s DIGITALLY SELF-CALIBRATED PIPELINE ALGORITHMIC ADC

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I. Introduction

This paper describes an algorithmic A/D converter which employs digital error correction and self-calibration. In an algorithmic A/D converter, variety of errors including capacitor mismatch, charge injection, and comparator offsets contribute inaccuracies giving differential nonlinearity (DNL) and integral nonlinearity (INL). Previous approaches of correcting capacitor mismatch in algorithmic converters include the ratio independent [1], reference refreshing [2], error averaging [3], which require additional clock cycles during the normal conversion, making the conversion slower. They also require two operational amplifiers per stage doubling the power and complexity. The analog calibration [4,5] requires a weighted capacitor array for the correction of each stage increasing the complexity and capacitive loading on op amps.

Although effective in converters employing weighted capacitor arrays such as successive approximation converters [6] and multi-step flash converters [7], conventional self-calibration techniques have not been amenable to algorithmic A/D converters due to the calibration required in the multiplicative factors.

In this paper, an approach is described that employs a nominal radix 2, 1.5 bit/stage conversion algorithm. Although a 1.5 bit/stage converter with capacitor ratio error cancellation has been previously reported [8], this technique is applicable only to non-pipelined single stage cyclic converter, hence slow. Furthermore, it requires a separate S/H amplifier, essentially doubling power and complexity. Another converter using the 1.5 bit/stage algorithm was reported recently [9]. However, this converter lacked self-calibration, and must be calibrated using highly accurate external D/A converter.

The technique discussed in this paper can be applied to any cyclic or pipelined algorithmic converters, does not require extra clock cycles during the conversion, and no additional analog circuitry is needed. The analog circuit is extremely simple, using one operational amplifier and two latches per stage. As will be shown in the next section, the 1.5 bit/stage algorithm makes a simple self-calibration possible in the digital domain. The combination of digital error correction and calibration removes any error due to capacitor mismatch, charge injection, comparator errors including offset and noise. Since the comparator decision error up to 1/4 full scale is corrected, the comparator can be strobed *before* the op amp has fully settled. Therefore the comparator decision delay does not cut into the conversion time. Moreover, a simple latch can be used as a comparator. For these reasons, *the converter presented here can operate at a maximum possible rate limited only by op amp settling times.*

The digital calibration converts the raw digital output into correct codes. In effect, it reassigns correct digital codes to the appropriate analog input voltage ranges, but does not create new decision levels. Therefore, the uncalibrated converter must provide all the necessary decision levels. In conventional algorithmic converters, this condition cannot be satisfied if capacitor mismatch, charge injection, or comparator offset is present. It can be shown that the 1.5 bit/stage algorithm *guarantees* this condition and makes a simple digital calibration possible.

Consider a fully-pipelined converter employing the 1.5 bits/stage algorithm. The input voltage to the i-th stage $V_i(i)$ is compared with two levels, V_A ($0<V_A<V_{REF}/2$) and V_B($-V_{REF}/2<V_B<0$) neither of which needs to be accurate. If the input is lower than V_B, the bit D(i) is set to -1. If the input is between V_B and V_A, the bit is set to 0, and if the input is higher than V_A, the bit is set to +1. The output voltage $V_o(i)$ is then produced:

$$V_o(i) = 2V_i(i) - D(i)V_{REF} \qquad (1)$$

where D(i) = +1, 0, or -1

It is important to note that in this algorithm, any comparator error including offset is eliminated, and the charge injection manifests itself only as overall input referred offset voltage. However, *the capacitor mismatch gives rise to DNL and INL and must now be corrected by the digital calibration.* The output voltage in (1) can be readily produced by a circuit shown in Fig. 1, which represents the i-th stage in a pipeline. Although a fully-differential configuration is preferred in practice, a single-ended version is shown in the figure for simplicity. In the fully differential circuit matching between V_{REF} and $-V_{REF}$ is not necessary. The ratio mismatch in nominally identical capacitors C1 and C2 are indicated as α_i. During the first phase of the clock, both C1 and C2 are connected to the input voltage V_{in} and the op amp is connected in the unity-gain mode as shown in Fig. 1a. During the next phase, C1 is connected to the output, and C2 is connected to V_{REF}, 0, or $-V_{REF}$ depending on the bit decision made in the first phase, as shown in Fig. 1b. The output voltage for the i-th stage is:

$$V_o(i) = 2(1+\alpha_i/2)V_i(i) - D(i)(1+\alpha_i)V_{REF} \qquad (2)$$

Equation (2) is identical to (1) if the mismatch α_i is zero. If α_i is known, it can be shown that the error can be canceled by adding a digital quantity $\varepsilon(i)$ to the digital output. where

$$\varepsilon(i)=\frac{\alpha_i}{2^i}[D(i)/2 - D(i+1)/4 - D(i+2)/8 - \cdots] \qquad (3)$$

The calibration of errors in other stages is done in the same manner. From (3) and similar equations for other stages, the correction term that corresponds to each bit D(i) is calculated during the initial calibration cycles, and stored in RAM. For a 12 bit converter, a 12-byte memory is sufficient. During the normal conversion, these correction terms are added to the conversion result to calibrate errors in all the stages that are calibrated. It should be noted that the calibration requires only digital additions or subtractions. In a fully-pipelined converter, α_i corresponds to the ratio error in each stage. In an N-stage cyclic converter, $\alpha_i = \alpha_{i+N}$ because the same stages are reused. For example, for a 2-stage cyclic converter, $\alpha_1 = \alpha_3 = \alpha_5 = \cdots$ and $\alpha_2 = \alpha_4 = \alpha_6 = \cdots$

The measurements the α's are done as illustrated in Fig. 2. First, 0V is used as an input to the i-th stage, which is digitized by the i-th and the following stages. The result gives the offset referred to the input of the i-th stage, $V_{OS}(i)$. Next, V_{REF} is sampled on C1, and 0V is sampled on C2 as shown

in Fig. 2a. By forcing the bit to 1, C2 is connected to V_{REF}, and C1 is connected to the output giving $V_{error} = \alpha_i V_{REF} + V_{OS}(i)$ as shown in Fig. 2b. This voltage is digitized by the following stages. By subtracting the offset measured previously, the value of α_i is obtained. It should be emphasized that *the measurement of V_{OS} and V_{error} does not depend on prior calibration of other stages*. This is because both V_{OS} and V_{error} are small quantities, and the following stage decisions will be 0, so the result will get multiplied by 2 without the addition or subtraction of V_{REF}, until the result reaches the final few stages where the bit decisions are 1's or -1's. The α errors in other stages therefore contributes only negligible gain error in the measurement of α_i. For this reason, *the calibration of each stage can be performed independent of other stages' calibration*. This also avoids accumulation of errors in the correction terms. The 1.5 bit/stage algorithm not only make the digital calibration possible, but also makes each stage calibration independent of other stages.

Experimental Results

A prototype 2-stage pipelined cyclic A/D converter employing the error-correction and self-calibration was implemented in a standard 1.6 μm CMOS technology. The output of the second stage is fed back to the first to obtain 14-bit uncalibrated digital outputs which are subsequently calibrated and truncated to yield 12-bit results. For each stage, a fully-differential 2-stage operational amplifier was used together with two simple latches as comparators. The logic circuit for the digital calibration was emulated by a computer program. The converter runs at a maximum of 4.2 MHz clock (600kS/s sampling rate) in the cyclic mode, at 45mW power. Fig. 3 shows the differential non-linearity (DNL) plot after calibration obtained by code-density measurments with the converter operating at full speed. The maximum DNL is shown to be ± 0.6 LSB's. The DNL peaks near the negative and the positive full-scales are due to the amplitude of the ramp which is slightly less than the full-scale.

Fig. 4 shows the integral non-linearity (INL) before and after calibration. Fig. 4a, the converter shows ±2.5 LSB's of INL before calibration. After calibration, it is improved to ±0.5LSB at 140kS/s, and to ±1LSB at 600kS/s respectively. The total input referred offset before calibration is 12 LSB's and is reduced to less than 1/2 LSB after calibration. The active die area is ~~0.5~~1.0 mm^2 (800 mil^2). Table I summarizes the experimental results.

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REFERENCES

[1] Li, P., et al., "A Ratio Independent Algorithmic Analog-to-Digital Conversion Technique," IEEE JSSC, vol. SC-19, Dec. 1984, pp. 1138-1143.

[2] Shih, C.-C., et al., "Reference Refreshing Cyclic Analog-to-Digital and Digital-to-Analog Converters," IEEE JSSC, vol. SC-21, Aug. 1986, pp. 544-554.

[3] Song, B.-S., et al., "A 12-bit 1-Msample/s Capacitor Error-Averaging Pipelined A/D Converter," IEEE JSSC, vol. SC-23, Dec. 1988, pp. 1324-1333.

[4] Ohara, H., et al., "A CMOS Programmable Self-Calibrating 13-bit Eight-Channel Data Acquisition Peripheral," IEEE JSSC, vol. SC-22, Dec. 1987, pp. 930-938.

[5] Lin, Y. M. et al., "A 13b 2.5MHz self-calibrated pipelined A/D converter in 3μm CMOS," IEEE J. Solid-State Circuits, vol. SC-26, pp. 628-636, Apr. 1991.

[6] Lee, H.-S. et al., "A Self-Calibrating 15 Bit CMOS A/D Converter," IEEE JSSC vol. SC-19, Dec. 1984, pp. 813-819.

[7] Lee, S.-H., et al., "A Code-Error Calibrated Two Step A/D Converter," IEEE ISSCC Digest of Tech. Papers, pp. 38-39, Feb. 1992.

[8] A CMOS RSD 13-b Cyclic RSD A/D Converter," IEEE JSSC vol SC-27, July 1992, pp. 957-965

[9] Jewett, R., et al., "A 12b 20MS/s Ripple-through ADC," IEEE ISSCC Digest of Tech. Papers, pp. 34-35, Feb. 1992

Resolution	12 bits
Sampling Rate	600kS/s
Power Supply	±2.5V
Input Range	±0.8 V differential
Power Dissipation	45mW
DNL	± 0.6LSB
INL	± 1LSB
Input Referred Noise	0.6LSB rms

Table I Summary of Experimental Results

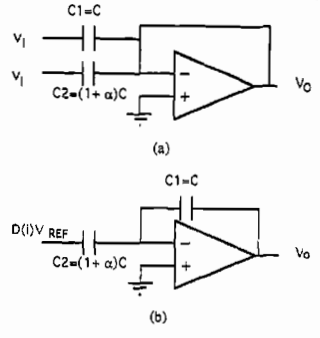

Fig. 1 Algorithmic Converter Stage: (a)Sampling Phase, (b)Multiply-by-2 Phase

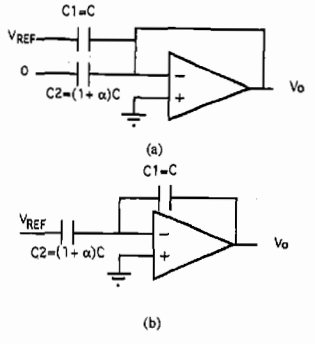

Fig. 2 Capacitor Ratio Error Measurement : (a)Sampling, (b) After Bit Decision is Forced to 1

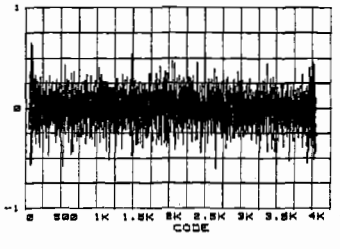

Fig. 3 Measured DNL after calibration (600 kS/s)

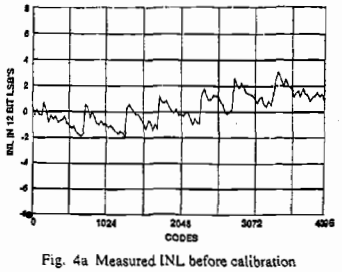

Fig. 4a Measured INL before calibration

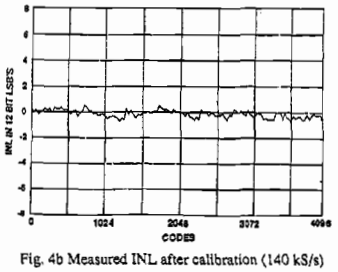

Fig. 4b Measured INL after calibration (140 kS/s)

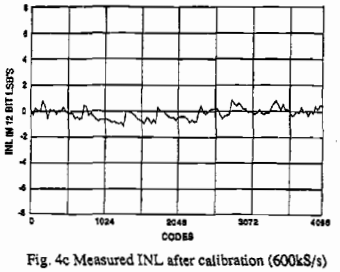

Fig. 4c Measured INL after calibration (600kS/s)