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A 1mW Delta-Sigma Modulator for Multichannel Applications

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1 Introduction

In recent years oversampling analog-to-digital converters have emerged as one of the most promising architectures for low frequency high resolution applications[1]. This technique has been shown to reliably provide high resolution without trimming or high precision components.

Oversampling converters consist of two main system blocks, the front end analog modulator and the digital decimator (Figure 1). The analog front end takes a bandlimited analog signal and produces a high frequency low resolution (usually 1-bit) output word. The area and power budget per channel of conventionally designed oversampled analog-to-digital converters have precluded their application from areas where a large number of low frequency signals need to be converted simultaneously. A new oversampled A/D design methodology is proposed to siginificantly cut the power and area budget per channel of an oversampled analog-to-digital converter. The design and implementation of this low power and area efficient delta-sigma modulator, which is the crucial building block for a multichannel system, is presented.

2 Design Methodology

In order to use the oversampled converters for processing very large number of channels simultaneously, we propose to optimize the analog and digital portions of the system separately. The *Multichannel Oversampled Data Acquisition System* (MODAS) is shown in Figure 2. The front end is a number of parallel multichannel analog modulator chips each of which contains (N) oversampled modulators. The output of this multichannel front end is processed by the multichannel decimator chips each of which is a highly multiplexed decimator architecture capable of processing the output of (M) analog front ends. The number of modulators (N) that can be designed on a single IC is heavily dependent on the design of very low power and area efficient modulator architecture which can be used as the core of the multichannel system.

In order to optimize the digital decimator portion we introduce the *extended baseband* design philosophy to alleviate the requirements on the digital decimator. The object of this approach is to relax the requirements of the digital filter such that it can be implemented in a single stage FIR structure which in turn allows the design of a highly multiplexed decimator capable of processing large number of analog front ends simultaneously. The extended baseband design trades off a slight increase in complexity of the analog front end to gain a large reduction in tap order of the digital FIR filter. Since the FIR tap order is inversely proportional to the transition width ($\Delta\Omega$) of the filter, by increasing the transition width we can reduce the tap order of the FIR filter. This implies that the front end modulator has to be designed not only to shape the noise over the signal baseband but also over the portion that would form the gradual transition width of the decimator filter (Figure 3).

This design methodology allows the separate optimization of both the analog front end and the digital decimator section. The separation of the decimator allows the analog front end multichannel system to be used for different applications by simply programming the new FIR coefficients to choose the required baseband and SNR for the particular application.

3 Modulator Design

To prove the feasibility of the approach described above a low power modulator has been designed to be used as the core of a multichannel data acquisition system. We have implemented a third order single loop modulator in a 2-micron CMOS process. The switch level block diagram of the modulator is shown in Figure 4. The modulator is a single loop architecture with distributed nature of the quantized feedback for increased stability characteristics[2][3]. One zero is at DC and the other two complex zeros are placed inside the baseband to improve the noise suppression within the baseband. The zero placement was chosen to extend the baseband as far as possible while maintaining the 14-bit resolution for signals below 1KHz. The modulator achieves (measured) a 14-bit signal to noise+distortion ratio over 1KHz baseband and 12-bit SNDR over the full 8KHz extended baseband while consuming only 1mW of power and 2 mm^2 area (2mm by 1mm). The output spectrum of the modulator, clocked at 500 KHz, is shown in Figure 5. The measured performance of the modulator is shown in Figure 6 and the full scale input refers to the maximum input before the loop goes unstable which is about 0.56 times the DAC reference. A fully differential class AB amplifier was used to implement the integrators to minimize the static power dissipation and still settle fast since the output current in a class AB amplifier is not limited by the quiescent current in the output stage. Switched capacitor common mode feedback was used to control the common mode level of the amplifiers. The complete amplifier and common mode

feedback schematic is shown in Figure 7. A fully differential latch with clocked output drivers was used as the single bit comparator in the modulator loop (Figure 8).

Power	0.94mW
Power Supplies	±2.5V
Full Scale Input Signal	5V Diff.
Area	2mm x 1mm

4 Conclusion

A new system level design methodology has been introduced to use the oversampled conversion schemes in areas where very large (hunderds to thousands) number of low frequency signals need to be converted simultaneously. A very low power and area efficient modulator design using a class AB amplifier has been presented. The modulator achieved 14-bit resolution over 1KHz baseband and performs at 12-bit level for the full 8KHz extended baseband using less than 1 milliwatt of power. This oversampled modulator can be used as the core of a multichannel data acquisiton system or for a single channel ultra low power telecommunication applications.

5 Acknowledgements

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References

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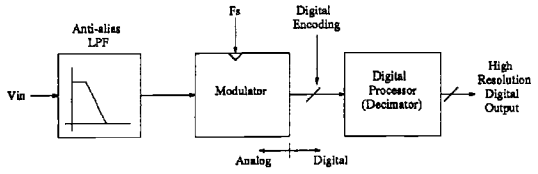
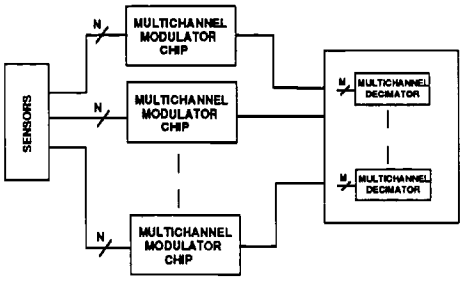
[2] W. L. Lee et al, "A Topology for Higher Order Interpolative Coders", pages 459-462, International Symposium on Circuits 1987.

[3] P. Ferguson et al,"An 18bit 20KHz Dual Sigma-Delta A/D Converter", pages 890-893, ISSCC 1991.



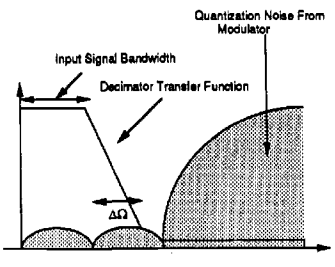
Oversampled Analog-to-Digital Converter

Figure 1



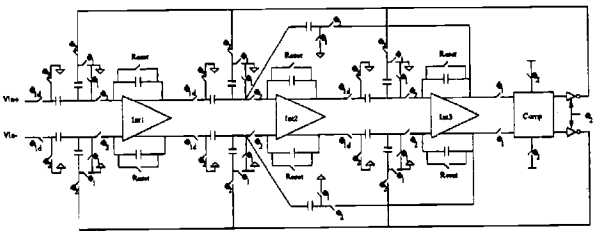
Multichannel Oversampled Data Acquisition System (MODAS)

Figure 2



EXTENDED BASEBAND DESIGN

Figure 3



Third Order Modulator

Figure 4

Fig5: Measured Performance

Input Signal : -6 dB
Signal Freq: 999.45 Hz
Clock Freq. : 500 KHz
Power : 0.94mW

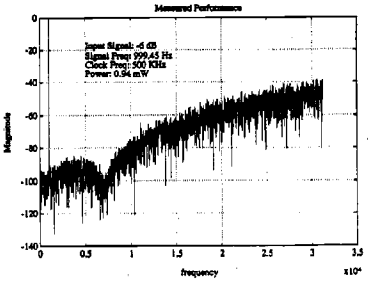


Figure 5

Fig6 : Measured Performance

S/(N+D) vs Input Mag

For 1K, 2K, 4K & 8K Basebands

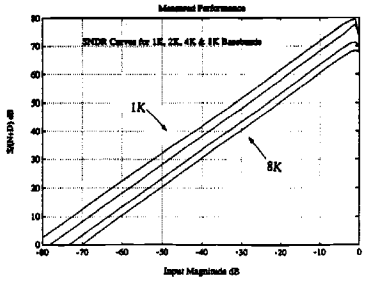
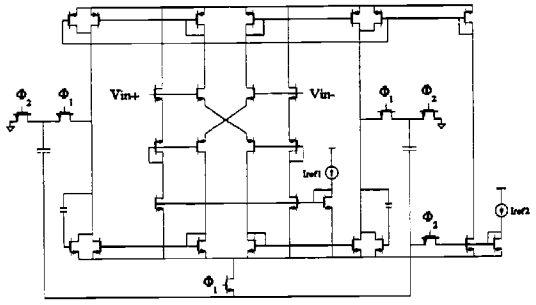
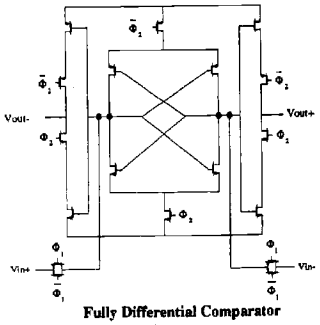


Figure 6



Fully Differential Class AB Amplifier

Figure 7



Fully Differential Comparator

Figure 8