TA 7.4: A High-Swing 2V CMOS Operational Amplifier with Gain Enhancement using a Replica Amplifier

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This open-loop gain enhancement circuit in 1.2μm CMOS does not require cascode or long-channel transistors, thus maximizing output swing and input common-mode range [1,2]. Since gain enhancement is achieved not by increasing output resistance, but by matching main and replica amplifiers, high effective open-loop gain is maintained even with resistive loads. This circuit can be used with any transconductance amplifier circuit. A basic 2-stage amplifier circuit demonstrates gain enhancement for low-voltage applications.

Consider a transconductance amplifier with a finite output resistance R_o. An inverting amplifier employing such a transconductance amplifier is shown in Figure 1 using capacitive feedback. The low-frequency open-loop voltage gain A_o of the transconductance amplifier is $A_o=gmR_o$. Assuming that the initial charge in both capacitors is zero, voltage v_O at dc is given by: $v_O=-\beta v_I/(1+(1+\beta)/A_o)$, where $\beta=C_S/C_F$

It can be seen that finite gain A_o produces an error corresponding to $(1+\beta)/A_o$, while an ideal amplifier with infinite A_o gives an output voltage of $-\beta v_I$.

Now, consider the circuit shown in Figure 2 where a replica amplifier RA, identical to the main amplifier MA, has the same feedback network connected around it. The coupling transconductance stage GM couples the input of the replica amplifier to the main amplifier (as will be shown in the next section, GM consists of a single transistor). For simplicity, assume that GM has infinite output resistance. (In practice, the effect of finite output resistance of GM is canceled by adding a dummy output stage to RA.) In this circuit, the output of the replica amplifier (v_O in the equation above) is close to the ideal output voltage within the error due to the finite gain. Thus, i'_X, the current injected into the main amplifier output by GM is already close to that needed to bring the output voltage of MA to an ideal output voltage. Therefore, the current needed from the main amplifier MA is small corresponding to the error between the ideal output and the output of the replica amplifier. The result is that only a small input voltage v_X of the main amplifier MA is needed to provide this error current. Hence, the effective open-loop gain of the main amplifier v_O/v_I is greatly increased. A quantitative analysis shows that the effective open-loop gain is increased by a factor of $A_o/(1+\beta)$. When the closed-loop gain β is small and A_o is large, this factor is potentially very large. In such cases, the actual improvement in the effective gain is limited by the matching between main and replica amplifiers. With a 5% mismatch, the improvement is limited to a factor of 20. In this case, resistive loading has little effect on the effective open-loop gain as long as the $(1+\beta)/Ao$ is less than the mismatch ratio, and if the same load resistor is placed at the output of the replica amplifier.

Another important fact is that coupling and replica amplifiers need not be identical to the main amplifier. Analyses similar to that above show that GM and RA can be scaled down in size and power without reducing the effectiveness of the gain enhancement.

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This gain-enhancement circuit relies on matched output voltages between main and replica amplifiers. Most feedback amplifiers with a relatively small closed loop gain β are suitable for this design. For a switched-capacitor integrator, however, a small capacitor switched between the replica integration capacitor and the main output is needed to prevent the replica amplifier output from running away.

A basic 2-stage operational amplifier circuit is chosen for high-output swing and input common-mode range higher than those of cascode designs. An example based on a 2-stage single-ended CMOS op amp is shown in Figure 3. Since both the first and the second stages are transconductance amplifiers, gain enhancement can be applied to either or both stages. For simplicity and lower noise, gain enhancement is applied to the second stage. The top half of the circuit is the main amplifier and the bottom half is the replica amplifier. MN4 serves as the coupling transconductance amplifier GM in Figure 2.

For both the main and replica amplifiers, the same ratio β is maintained between Z_s and Z_f. Matching of output resistance between main and replica outputs is accomplished by a circuit consisting of MNX4, MNX5, MPX5 and MPX6 to make the outputs of main and replica amplifiers identical. The CMOS operational amplifier of the same design shown in Figure 3 is implemented in 1.2μm CMOS. Only minimum-length transistors are employed for speed and output swing with the exception of MP4 and MPX4 that are 1.8μm long. The test circuit shown in Figure 4 is used to measure performance. For the main amplifier a total of 27pF load capacitance is used. For the replica amplifier, the total load capacitance is approximately 10pF. Figure 5 shows the step response of the test circuit shown in Figure 4. 1% settling time is 54ns, approximately 50% longer than without gain enhancement. The increase can be minimized by making the bandwidth of the replica amplifier higher than that of the main amplifier. This is relatively easy because the replica amplifier does not have significant capacitive load. In the present design, however, the same bandwidth is used for both amplifiers.

Table 1 summarizes measured performance. The effective dc gain is increased by a factor of approximately 18 with no load resistor, and a factor of 58 with a 1kΩ load. Power dissipation and die area are approximately twice those without the enhancement. However, the power and the area increase can be reduced by scaling down the replica amplifier. This was not done in this design for simplicity. The amplifier retains dc gain even with a 1kΩ load resistor connected to both main and replica amplifiers. Figure 6 is a die micrograph.

References

[1] Li, P. W., M. J. Chin, P. R. Gray, R. Castello, "A Ratio Independent Algorithmic Analog-to-Digital Converter", IEEE J. Solid-State Circuits, vol. SC-19, pp. 1138-1143, Dec. 1984

[2] Bult, K., G.J.G.M. Geelen, "A Fast Settling CMOS Op Amp for SC Circuits with 90dB Gain", IEEE J. Solid-State Circuits, vol. SC-25, pp. 1379-1384, Dec. 1990.

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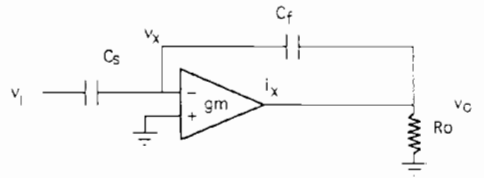

Figure 1: Inverting amplifier.

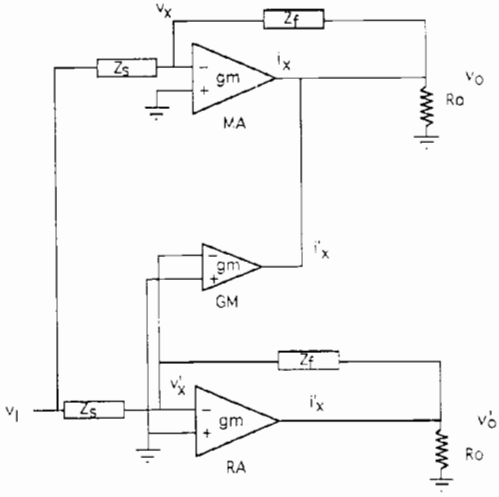

Figure 2: Gain enhancement with replica amplifier.

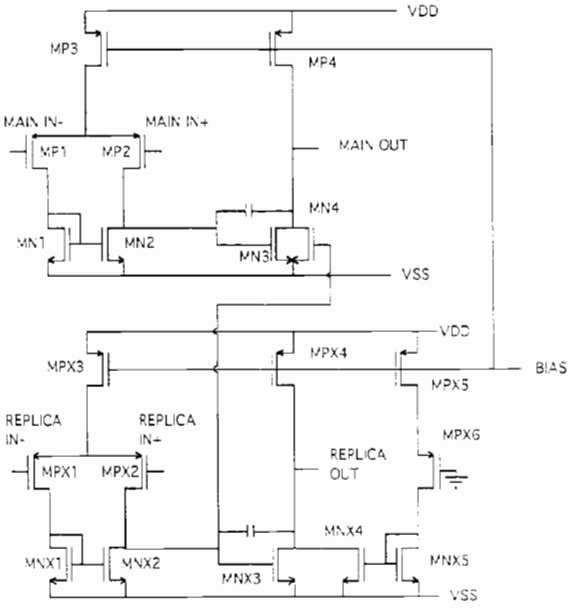

Figure 3: 2-Stage single-ended op amp with gain enhancement.

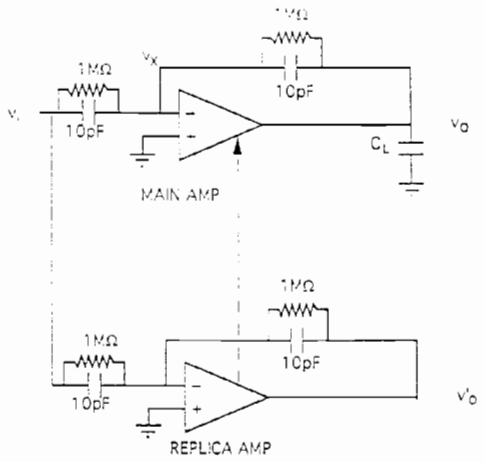

Figure 4: Operational amplifier test circuit.

Enhancement	Without	With
Power supply voltages	+1.0, -1.0	+1.0, -1.0
Output swing	100mV from either rail	
dc gain: no load	810	10,600
1kΩ resistive load	200	10,500
Power dissipation	4mW	9mW
Settling time (1%)	55ns	55ns
Gain-bandwidth	63MHz	63MHz
Load capacitance	27pF	27pF
Die area	0.34mm²	0.61mm²

Table 1: Summary of measured performance.

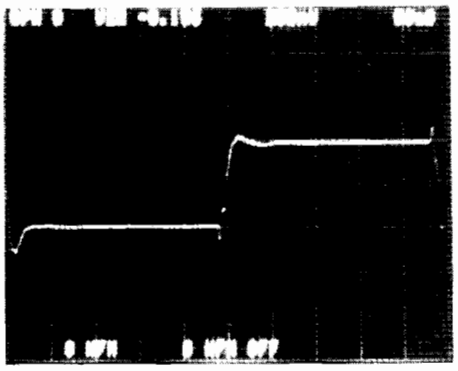

Figure 5: Step response with gain enhancement (horizontal: 50ns/div.; vertical: 200mV/div.).

Figure 6: See page 273.

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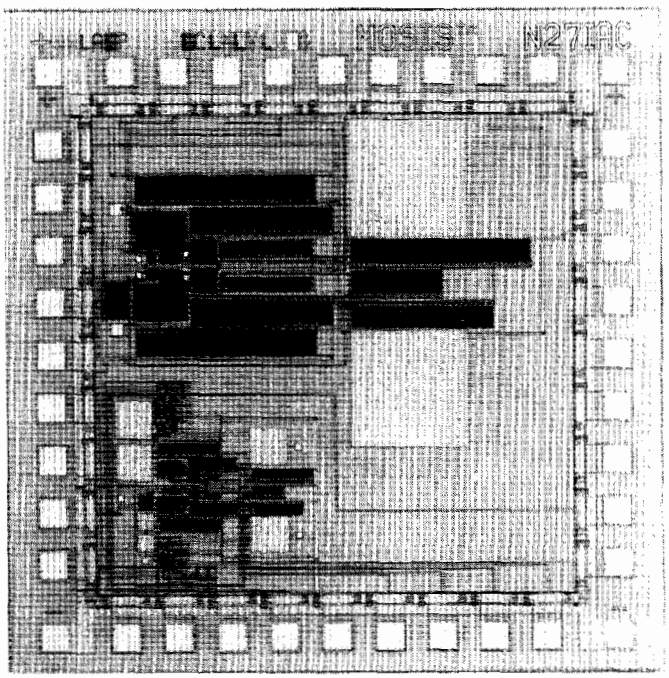

Figure 6: Die micrograph.

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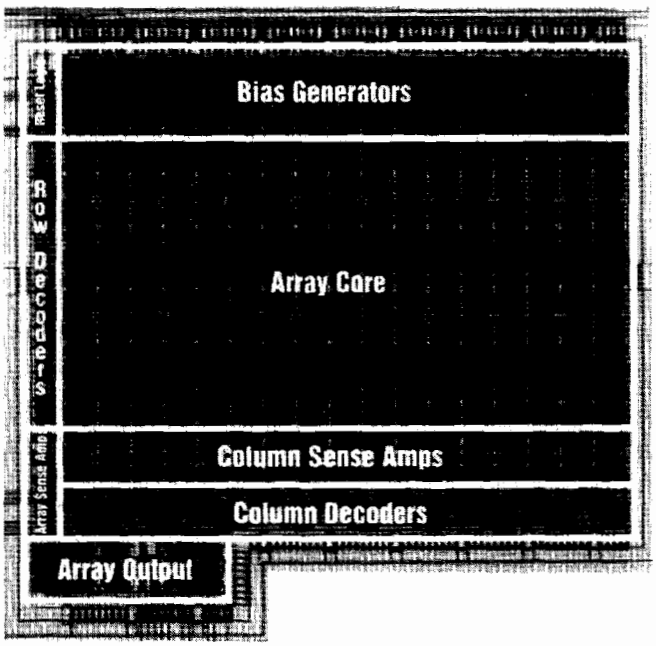

Figure 4: Die micrograph of array oscillator.