CMOS RESISTIVE FUSE CIRCUITS

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INTRODUCTION

In this paper, we present simple CMOS circuits, each of which functions as a linear resistor within a predetermined range of the voltage across it, and as an open circuit outside that range. The circuits have been fabricated in a standard 2μm CMOS process in a silicon area of 70μm X 90μm, and operate at a single 5V supply.

In the early stage of vision processing, it is desirable to smooth out small variations of intensity in the image. A spatial low-pass filter which performs a Gaussian or binomial convolution of the image has been used for image smoothing. An interesting implementation of such a spatial low-pass filter is a resistive grid shown in Fig. 1, where V(i,j) is the voltage proportional to the intensity at the pixel (i,j), and V'(i,j) is the smoothed data. It can be shown that V'(i,j) is the discrete spatial convolution of V(i,j) with an exponential function [1]

$$f(x) = \frac{1}{2\alpha} \exp(-\alpha|x|)$$

where

$$\alpha = \sqrt{\frac{R_h}{R_v}}$$

Unfortunately, such smoothing blurs the edges of the image which makes the edge detection more difficult. Resistive fuse networks have been proposed where the vertical resistors are replaced by a resistive fuse to overcome this problem [2]. For small intensity variations, the resistive fuse functions as a linear resistor, thus smoothing the image as in the conventional resistive grid. However, when there is a large intensity difference between the adjacent pixels, the resistive fuse breaks, becoming essentially an open circuit. Smoothing is discontinuous where the fuse breaks, and the edge is preserved. Note that the resistive fuse is a repairable fuse, returning to the linear resistor state if the voltage is reduced within the limit (off-voltage). Previous implementations of resistor fuses require a large number of MOS transistors (at least 33 transistors per fuse) [2], or process modifications to yield depletion mode NMOS and PMOS transistors, and offer no control over the linear resistance or the off-voltage [3]. Here, we present two simple circuits using a standard CMOS process which use only 7 and 11 small size transistors per fuse. Furthermore, the linear resistance and the off-voltage can be individually controlled which offers the flexibility of controlling the spatial constant α and the threshold of smoothing.

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Fig. 2 shows the new 7-transistor resistive fuse circuit where node 1 and 2 are the two terminals of the resistive fuse. The saturation currents I_{DS5} and I_{DS6} are made somewhat larger than half of the tail current I;

$$I_{DS5} = I_{DS6} = \frac{I + \Delta I}{2}$$

When the voltage across the fuse V1-V2 is small, the voltages V3 and V4 are pulled up near the positive rail because the saturation currents of M5 and M6 are larger than the drain currents of M1 and M2, which are approximately I/2 each. M5 and M6 stay in the triod region, and they function as linear resistors. The series combination of these two linear resistors is the equivalent resistance between the two terminals of the fuse;

$$R_{EQ} = [k_{5,6}(V_{GS5,6} - V_T)]^{-1}$$

where $k_{5,6} = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_{5,6}$

As V1 is raised with respect to V2, more current is steered to M1. When the drain current of M1 exceeds $\frac{I + \Delta I}{2}$, V3 is quickly pulled down near the source potential of M1, turning M3 off. Since the circuit is symmetric, the same thing happens in the opposite direction, also. The off-voltage V_{OFF} which is the voltage across the fuse when either M3 or M4 turns off can be found to be;

$$V_{OFF} = \pm \frac{\sqrt{I + \Delta I} - \sqrt{I - \Delta I}}{\sqrt{2k_{1,2}}}$$

Thus, it can be seen that the off-voltage can be controlled by controlling either I or ΔI. Typically, this control is global so that the V_{BIAS1} and V_{BIAS2} are common to all the fuses in the network.

The drawback of the simple 7 transistor circuit in Fig. 2 is the sensitivity of the linear resistance R_{EQ} to the common-mode voltage $V_{CM} = \frac{V1 + V2}{2}$ across the fuse. Since V_{GS5} and V_{GS6} varies directly with V_{CM}, R_{EQ} is a linear function of V_{CM} rather than constant. In some applications such variations may be tolerable, while less common-mode sensitivity is desired in other applications. The circuit shown in Fig. 3 reduces the common-mode sensitivity greatly. In this circuit, a linear resistor R is inserted between M3 and M4. The resistance R is made much larger than the ON-resistances of M3 and M4, so that M3 and M4 are essentially switches. Therefore, the linear resistance is constant at R. The difficulty of this circuit is that the linear resistor R is physically very large for it to be much larger than the ON-resistance of M3 and M4. Also, once the circuit is built, the linear resistance cannot be varied.

In the 11-transistor circuit shown in Fig. 4, the linear resistor is replaced by an NMOS transistor M7 biased at constant $V_{GS} - V_T$. For zero differential voltage across the fuse, V1 = V2 = V6 assuming the same current density for M1, M2, and M9. Then, $V_{GS7} - V_T = V_{GS8} - V_T = \sqrt{\frac{I_1}{k_8}}$

Thus, the linear resistance R_{EQ} is;

$$R_{EQ} = R_{ON7} = \left(k_7\sqrt{\frac{I_1}{k_8}}\right)^{-1} \qquad (1)$$

Note that R_{EQ} is independent of the common-mode voltage, and is controllable by adjusting I_1.

EXPERIMENTAL RESULTS

The 11-transistor circuit in Fig. 4 is fabricated in a standard 2 μm p-well CMOS process through MOSIS. Fig.5

shows a typical i-v characteristic at two different current levels. For a factor of 10 change of I and ΔI, the linear resistance changes from 2 MΩ to 300 kΩ or by a factor of 6.7. This significantly more than a factor of 3.16 predicted by (1). The discrepancy is because the transistors are being operated in or near the subthreshold region rather than the square-law region assumed in deriving (1). Fig. 6 shows the controllability of V_{OFF}. By varying ΔI from 200 nA to 900 nA, V_{OFF} is varied from 30 mV to 110 mV. Fig. 7 shows the common-mode sensitivity of the linear resistance and the off-voltage. For a 1.5 V variation of the common-mode voltage, ± 25% variations of R_{EQ} and V_{OFF} are observed. This sensitivity is due to the finite output resistance of the MOS transistors. The slight raggedness of the characteristic near the origin is due to the extremely small current levels (1nA) approaching the resolution limit of the instrument used in the measurement.

ACKNOWLEDGEMENT

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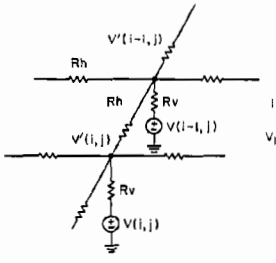

Fig. 1 2-D Resistive Grid

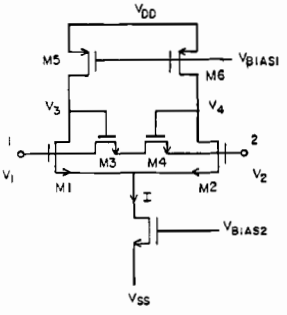

Fig. 2 A 7 Transistor Resistive Fuse Circuit

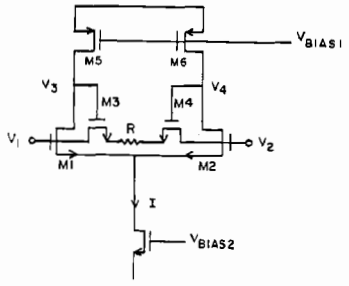

Fig. 3 An Improved Resistive Fuse Circuit

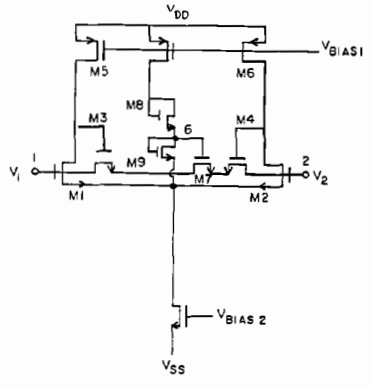

Fig. 4 An 11-Transistor Resistive Fuse Circuit

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[3] Horn, B.K.P., Lee, H.-S., Poggio, T. Sodini, C.G. Wyatt,J., "The First Year of the MIT Vision Chip Project" *VLSI Memo, No. 90-605* MIT, Cambridge, MA, Oct. 1990

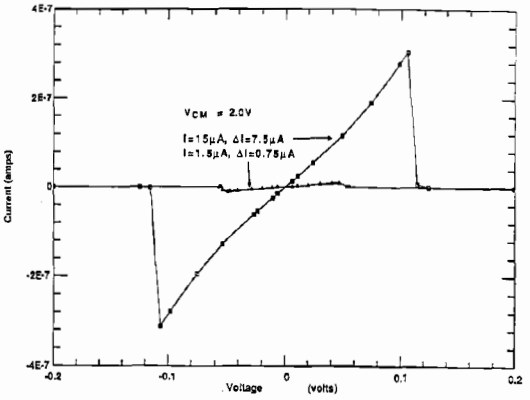

Fig. 5 I-V Characteristic of 11-Transistor Resistive Fuse

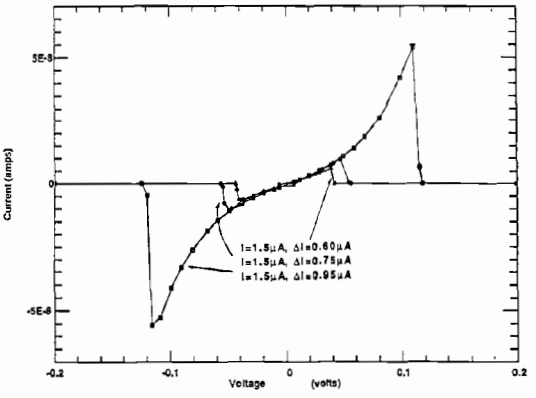

Fig. 6 Variability of V_{OFF}

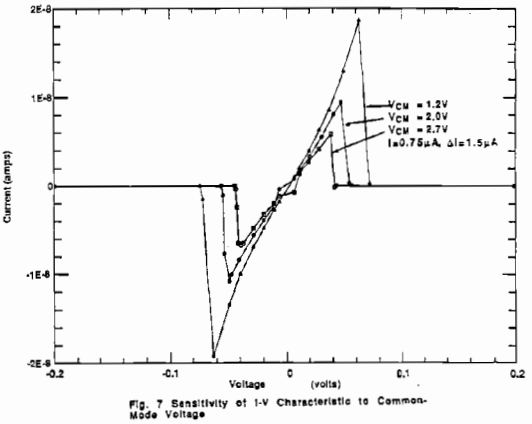

Fig. 7 Sensitivity of I-V Characteristic to Common-Mode Voltage