WP 4.2: A 15b 1Ms/s Digitally Self-Calibrated Pipeline ADC*

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The primary accuracy limitations of a switched-capacitor pipeline ADC are capacitor mismatch, charge injection, finite operational amplifier gain and comparator offset. Previous 1b-per-stage ADCs remove some of these errors by using extra clock cycles [1-3]. Although analog calibration does not require extra clock cycles during normal conversions, for pipeline ADCs where many stages are calibrated, the added complexity and capacitive load are significant [4]. This paper presents a digital calibration technique based on radix 1.93. The digital calibration presented here may be applied to pipeline or cyclic ADC architectures. An important advantage of this design is that calibration is performed in the digital domain so no extra analog circuitry, such as weighted capacitor arrays, and no extra clock cycles are needed. This calibration automatically accounts for capacitor mismatch, capacitor non-linearity, charge injection, finite op-amp gain and comparator offset.

Unlike analog calibration, digital calibration alone does not correct or create analog decision levels. Therefore, the uncalibrated ADC must provide decision levels spaced no greater than 1LSB at the intended resolution. In 1b/stage pipeline ADCs with nominal gain of 2, missing decision levels result when the input of any stage exceeds full scale due to capacitor mismatch, capacitor non-linearity, charge injection and comparator offset. Missing decision levels can be eliminated, however, by using gain less than 2 and 2-3 more stages of pipeline giving enough redundancy in the analog decision levels. The missing codes with gain less than 2 are eliminated by digital calibration.

For each stage of a 1b/stage ADC, the decision level is placed at 0V, resulting in the residue plot shown in Figure 1. With the radix of 1.93, missing codes result at the carry-transition point at the center. Noting that S1 and S2 correspond to the same input voltage of 0V, these missing codes can be eliminated by making the digital output codes for the points S1 and S2 to be consecutive. This is accomplished by the following calibration algorithm for each stage:

$$Y = X, \text{ if } D = 0 \quad (1)$$

$$Y = X + S1 - S2 + 1, \text{ if } D = 1 \quad (2)$$

where Y is the calibrated code, X is the raw code and D is the bit decision. From equation 2, it is seen that two quantities S1 and S2 must be measured for each stage being calibrated. S1 is measured with 0V as input and D = 0. S2 is measured with 0V as input and D = 1. Since calibration aligns points S1 and S2 using measured values, calibration automatically accounts for capacitor mismatch, charge injection and finite op-amp gain. Capacitor non-linearity causes only integral nonlinearity (INL) error, not differential nonlinearity (DNL) error. Comparator errors up to ±0.8% of full scale have no effect on conversion accuracy. Due to the nominal radix of 1.93, the calibrated output code has non-unity nominal gain, easily compensated for elsewhere in the system. Only digital addition and subtraction are needed for calibration and only two calibration constants need be stored for each calibrated stage.

The prototype ADC consists of an input sample-hold amplifier (SHA) and 17 stages of pipeline for 15b resolution. Each of the 17 stages uses a multiply-by-two (MX2) amplifier and a comparator. The first 11 stages of the pipeline are calibrated and have a nominal gain of 1.93 for decision-level redundancy. The last 6 stages are uncalibrated and have a nominal gain of 2. A single-ended schematic of a MX2 amplifier for the even numbered stages is indicated in Figure 2a during the sample phase and in Figure 2b during the amplify phase. Capacitors C1 and C2 are nominally equal. A small capacitor C3 is added to reduce nominal gain to 1.93. Nominally, C3 = 0.035C1. The previous bit decision D determines whether Vref or -Vref is subtracted. Figure 3 shows the schedule for the ADC using two-phase, non-overlapping clocks. The comparator is strobed at the end of the amplify phase for the respective stage.

Calibration starts from the last stage to be calibrated, namely the 11-th stage. The 11-th stage together with the following 6 uncalibrated stages is operated as a 7b ADC with 0V as input. From the resulting digital output codes, calibration constants S1 and S2, as in equation 2, for the 11-th stage are obtained and stored in memory. Next, the calibration proceeds to the 10-th stage and up in a similar manner until the first stage is calibrated. Quantization and truncation errors are avoided by averaging calibration data without truncation.

The fully-differential pipeline ADC is implemented in an 11V, 4GHz, 2.4μm BiCMOS process. The operational amplifier is a 2-stage design with a 100MHz unity gain bandwidth and a 125dB d-c gain [5]. Although digital calibration automatically removes errors from finite op-amp gain, high op-amp gain eliminates recalibration if the gain drifts. The comparator uses 2 pre-amplifiers in cascade driving a latch. For offset below ±0.8% full scale, offset cancellation is employed in the pre-amplifiers. The ADC uses external logic and software to perform addition and subtraction for the digital calibration algorithm. The chip is designed for a maximum sampling rate of 8Ms/s. However, the present experimental set-up is limited to 1Ms/s.

Figure 4 shows a measured FFT plot of output with a 9.8756kHz sine wave input. The signal-to-distortion ratio (SDR) is 88.1dB. Figure 5a is a plot of measured DNL at 15b resolution. The peak DNL is within ±0.5 LSB. In Figure 5b, DNL is plotted for 16b resolution. Maximum DNL increases to approximately ±0.85 LSB. Although capacitance and power can be scaled down for later stages of the pipeline, identical designs are employed for all 17 stages and SHA for simplicity. No attempts were made to optimize die area. Figure 6 shows a micrograph of the 9.3x8.3mm² ADC containing 5955 components. The chip has 4V input range and dissipates 1.8W with ±4V supply (reduced from ±5V on some parts due to changes in process ground rules.)

Acknowledgments

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References

[1] Li, P. W., et al., "A Ratio Independent Algorithmic Analog-to-Digital Conversion Technique", IEEE J. of Solid-State Circuits, vol. SC-19, no. 6, pp. 1138-1143, Dec. 1984.

[2] Shih, C-C., et al., "Reference Refreshing Cyclic Analog-to-Digital and Digital-to-Analog Converters", IEEE J. of Solid-State Circuits, vol. SC-21, pp. 544-554, Aug. 1986.

[3] Song, B-S., et al., "A 12-bit 1-Msample/s Capacitor Error-Averaging Pipelined A/D Converter", IEEE J. of Solid-State Circuits, vol. SC-23, no. 6, pp. 1324-1333, Dec. 1988.

[4] Ohara, H., et al., "A CMOS Programmable Self-Calibrating 13-bit Eight-Channel Data Acquisition Peripheral", IEEE J. of Solid-State Circuits, vol. SC-22, pp. 930-938, Dec. 1987.

[5] Karanicolas, A. N., et al., "A High Frequency Fully Differential BiCMOS Operational Amplifier," IEEE J. of Solid-State Circuits, vol. 26, no. 3, pp. 203-208, Mar. 1991.

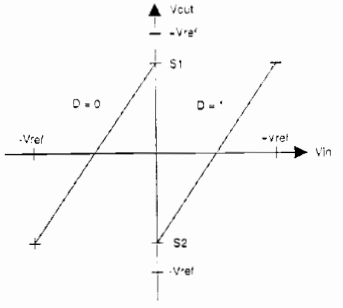

Figure 1: Residue plot of a MX2 stage.

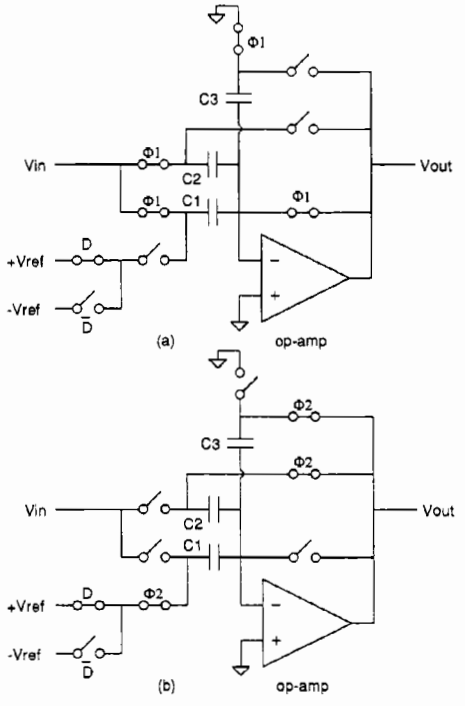

Figure 2: Single ended version of a MX2 amplifier for an even-numbered stage in (a) sample phase (b) amplify phase.

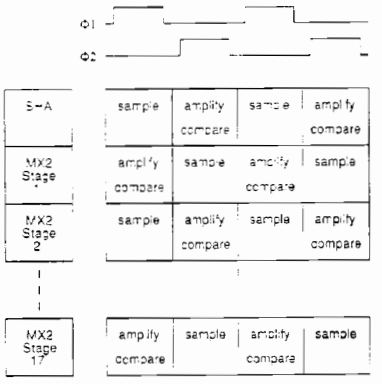

Figure 3: Pipeline ADC schedule.

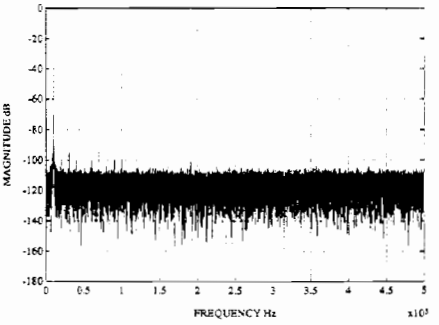

Figure 4: Measured FFT plot.

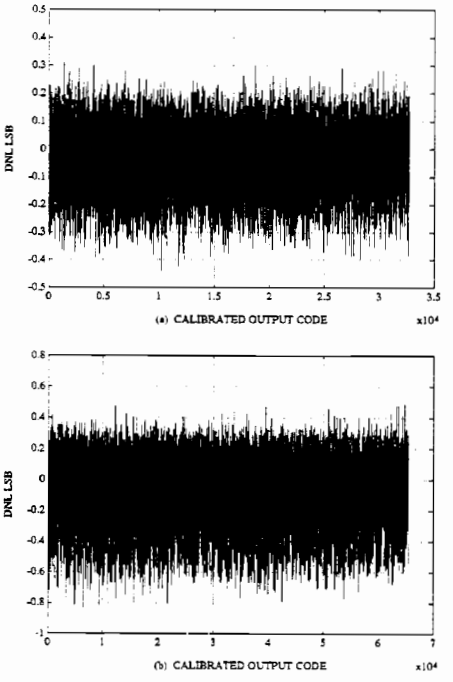

Figure 5: Measured differential non-linearity at (a) 15b, (b) 16b.

Figure 6: See page 263.

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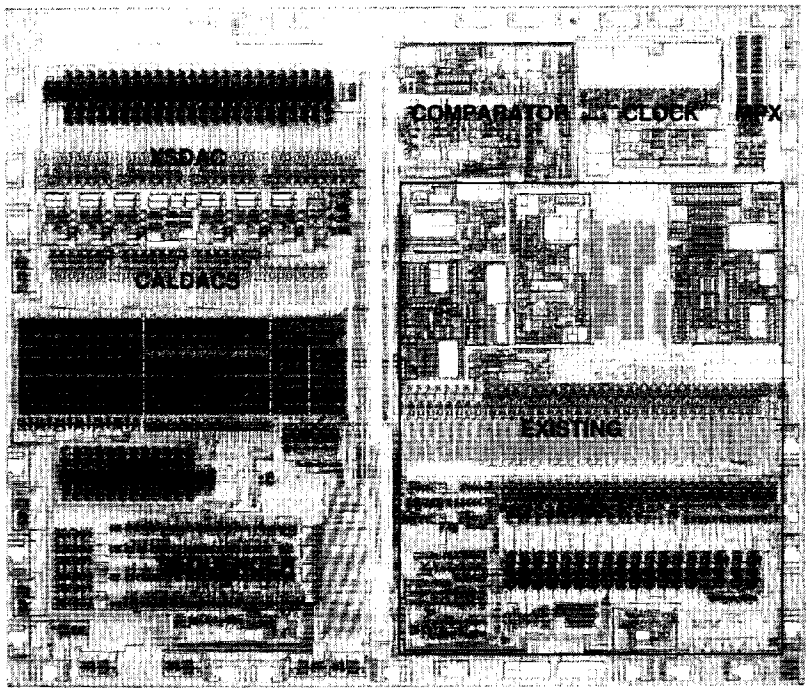

Figure 7: Chip micrograph.

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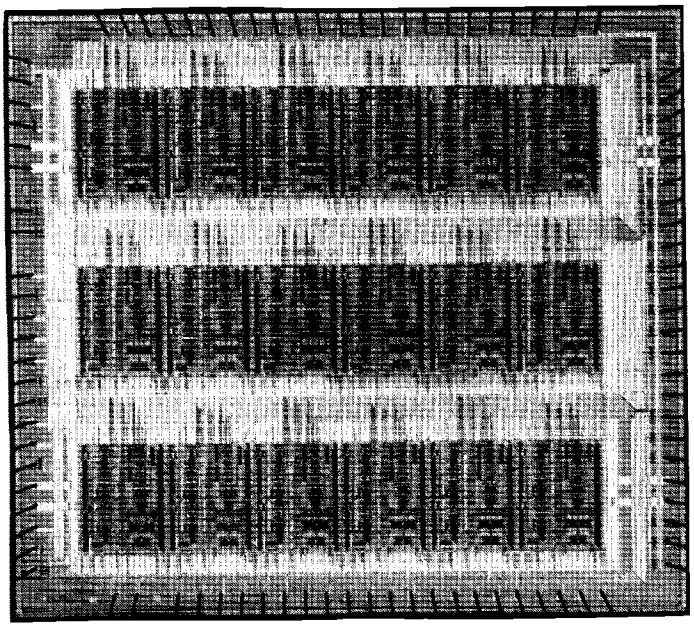

Figure 6: Pipeline ADC micrograph.