MP 3.3 A Nyquist-Rate Pipelined Oversampling A/D Converter*

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Oversampling and noise-shaping techniques, such as ΣΔ modulation, have an inherent tradeoff between accuracy and speed, whereby resolution in amplitude is at the expense of resolution in time. Because their internal circuits must operate over many clock cycles to produce a single result, they have limited data rates and power dissipation is a concern. Much attention has been focused on improving the speed and power of ΣΔ analog-to-digital converters (ADCs) by use of higher-order modulators, multi-bit feedback, and multi-bit architectures with single-bit feedback [1,2]. However, data rates remain limited to less than a few MHz and are not easily extended.

A pipelined oversampling architecture circumvents this speed-resolution tradeoff by performing spatial, rather than temporal, oversampling. It combines the high resolution of ΣΔ techniques with the high speed of pipelined converters so that both of these attributes are simultaneously achievable. A conventional ΣΔ ADC, shown in Figure 3.3.1a, includes a single modulator operating at a speed much greater than the Nyquist rate. A time sequence of many outputs is processed in the decimator for each result. In contrast, a pipelined oversampling converter (POSC), shown in Figure 3.3.1b, performs oversampling in space. Its modulator and decimator loops are unraveled into a pipeline so that consecutive operations occur along consecutive stages, rather than within a single piece of hardware. Incoming signals are sampled by the first stage, processed by a ΣΔ algorithm along the pipeline, and a digital result is produced by the final stage. Since a POSC computes a new result at every cycle, its output data rate equals its input sampling rate, and no higher-speed circuits are required. On the other hand, its resolution is a function of pipeline length. These attributes can be independently adjusted within the constraints of a given process technology.

A POSC resembles a conventional ΣΔ converter in its quantization process. However, from an input-output perspective it is indistinguishable from a Nyquist-sampling converter because, like the device in Reference 3, each input sample is processed independently from its neighbors. This architecture supports input bandwidths up to half the pipeline clock rate and is suitable for presampled or clocked signals. Like any Nyquist-sampling ADC, the advantages of Nyquist sampling in a POSC occur for the price that its input must be bandlimited with an anti-alias filter. A POSC achieves higher speed at the cost of additional hardware. However, all of its inputs exercise the same circuit path and it is not a parallel-channel architecture.

Although the POSC architecture is not specific to any technology, such a device is most practically accomplished using a combination of charge-coupled device (CCD) and CMOS circuits. CCDs make pipelines with hundreds of stages feasible by contributing sample-and-hold, delay, transfer, and integration operations that are highly accurate, low power, simple and compact. CMOS also plays a vital role by providing digital logic, CCD support circuitry, and other analog functions such as comparison. Most CCD operations are fully depleted and are not subject to thermal noise or coupling from clocks or the substrate. This attribute makes high signal integrity possible throughout hundreds of transfers and amidst noisy digital circuits and also helps to keep power low. In other non-depleted CCD operations, thermal noise decreases with decreasing capacitance so power and noise are reduced.

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Figure 3.3.2a introduces a 2nd-order pipelined ΣΔ algorithm. To accommodate pipelining, each operation includes a delay in its forward path. The decimator consists of three cascaded accumulators that are reset at the beginning and truncated at the end of the pipeline. The input to a POSC has a spectral distribution that is signal-independent and precisely known to be constant along the length of the pipeline. Because of this, matched-filtering can be applied. The decimator shown is nearly a matched filter for this configuration. Multi-bit feedback is preferable for a POSC since matching requirements are independent of the number of bits in each DAC. The configuration shown has a 5b feedforward ADC and utilizes a feedback technique similar to that in Reference 2. The two most significant bits are fed back and the remaining three are used in the decimator to digitally cancel truncation error.

A prototype device demonstrates pipelined oversampling. Its modified architecture, shown in Figure 3.3.2b, computes an identical ΣΔ algorithm to that in Figure 3.3.2a but is more easily implemented. DAC operations are relocated from before, to after, the first integrator so that the first stage of integration occurs digitally. The first integrator requires no hardware since its values are already present in signals $d1$, w, and stage number n. The prototype algorithm is implemented as shown in Figure 3.3.3. A two-stage approach is adopted, with a non-oversampling front end and a pipelined oversampling back end. The front end, consisting of a one-bit-per-stage block, provides a coarse estimate of the incoming signal and generates a residue quantity that is passed forward to the remainder of the converter. The 12-stage oversampling pipeline is divided into even and odd halves and every signal is passed simultaneously through both of them. Decimator signal, $d3$, from the last stage produces the final converter result. Contents of the nth pipeline stage are shown in Figure 3.3.4. Analog summation is achieved by combining charges in a CCD well. DAC functions are by pulsing an array of capacitors and integrating their displacement current in a CCD well. The ADC nondestructively senses CCD charges and performs one-bit-per-stage quantization.

This prototype demonstrates that high-performance CCD devices are achievable using only standard CMOS processing. The prototype is fabricated in a commercial 1.2μm 2-poly 2-metal CMOS process with no CCD provisions. Overlapping CCD structures use parasitic 2nd-poly transistors over gate oxide. Channel regions for the CCDs are identical to those for MOS devices. Even with such surface channel CCDs, charge transfer inefficiency does not limit device resolution. Despite concerns about overlapping gate structures in this non-planarized process, the yield is over 90%.

The prototype modulator, decimator, and all necessary support logic are integrated onto a single 47mm^2 chip. Major functional blocks are indicated on the die photograph in Figure 3.3.5. Testing uses an automated ADC testbed. Measured performance is listed in Table 3.3.1. Measurements are at 18MHz sampling rate with an input sinusoid near 8MHz. Performance is unchanged for lower-frequency inputs. Spectral response, DNL, and INL are shown in Figure 3.3.6. The presence of higher-order harmonics was anticipated for this prototype due to its two-stage approach. Prototype power scales linearly with frequency since all of its circuits are strictly dynamic. At full speed the device operates from 5V, 4V, and 3.3V for analog CMOS, CCD, and digital CMOS, respectively and consumes 324mW. At 10MHz, voltages may be lowered and power is reduced to 122mW. Of the total power, 65% is due to CMOS modulator circuits, 20% is due to CCD clock drivers, and 15% is due to the decimator. Substantial improvements in power, speed, and area may be achieved for future generations of the POSC architecture by scaling process geometries below 1.2μm.

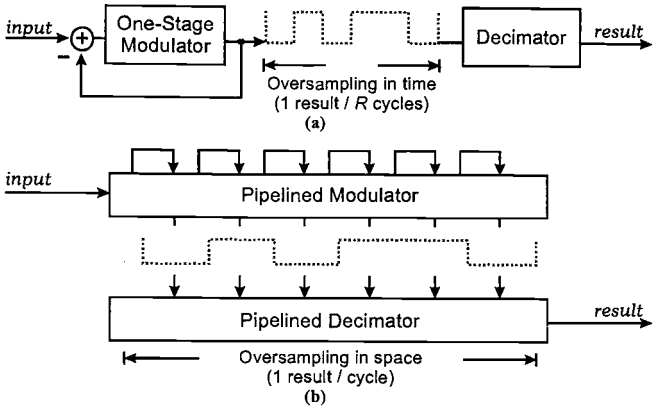

Figure 3.3.1: **Oversampling comparison.**
(a) Temporal: many cycles per result.
(b) Pipelined: one result per cycle.

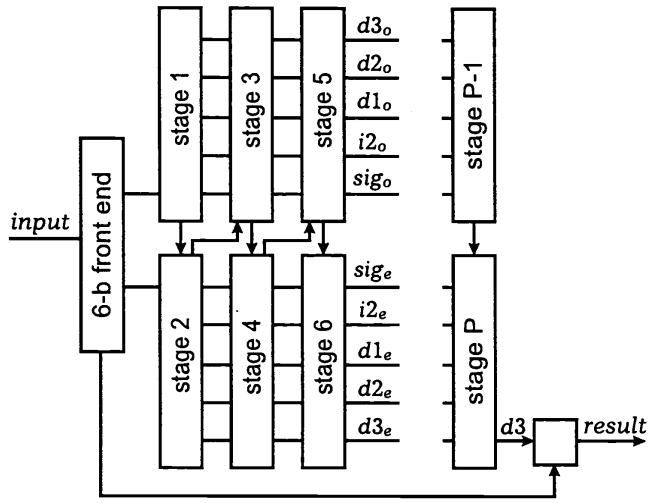

Figure 3.3.3: **Prototype with even and odd pipelines.**
Signals pass through both simultaneously.

Dynamic Range	78 dB
Peak SNR	74 dB
Data Rate	18 MSPS
Differential Nonlinearity	±0.15 LSB @ 13 bits
Integral Nonlinearity	±1.0 LSB @ 13 bits
Peak SFDR	78 dB
Peak SNDR	71 dB
Power @ 18 MHz	324 mW
Power @ 10 MHz	122 mW
Analog Supply Voltage	5 V
Digital Supply Voltage	3.3 V
Process	Commercial CMOS
Design Rule	1.2 μm
Yield	22 of 24

Table 3.3.1: Summary of measured prototype performance.

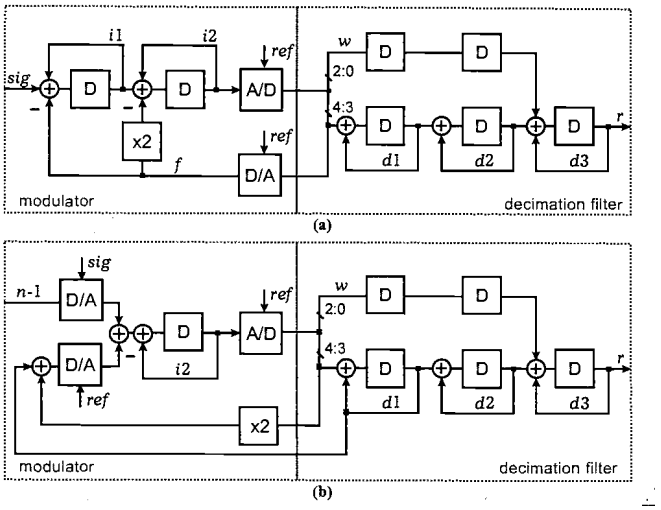

Figure 3.3.2: **Pipelined ΣΔ algorithms shown in cyclic form.**
(a) Analog integration .
(b) Digital integration used for prototype.

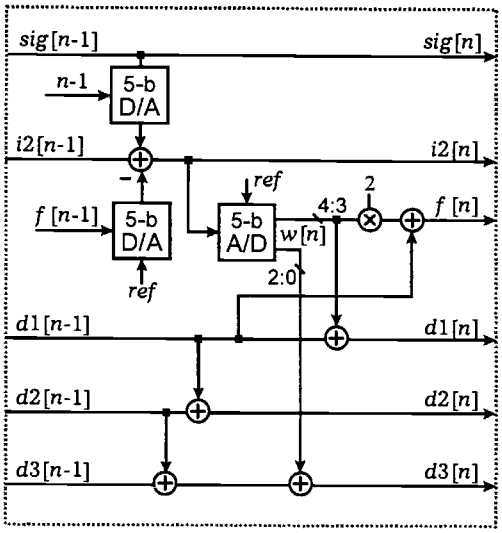

Figure 3.3.4: **Contents of nth pipeline stage of prototype.**
Delays and differential signals not shown.

Acknowledgments

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References

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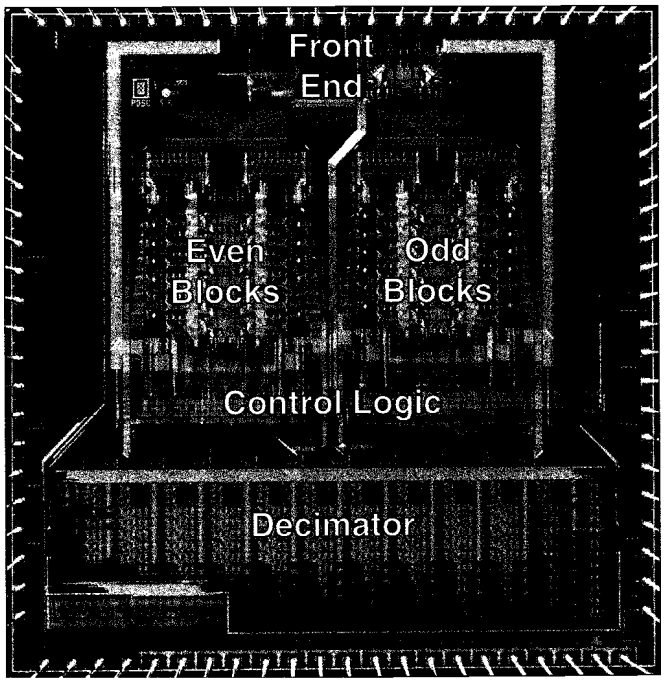


Figure 3.3.5. Micrograph and functional breakdown of POSC prototype.

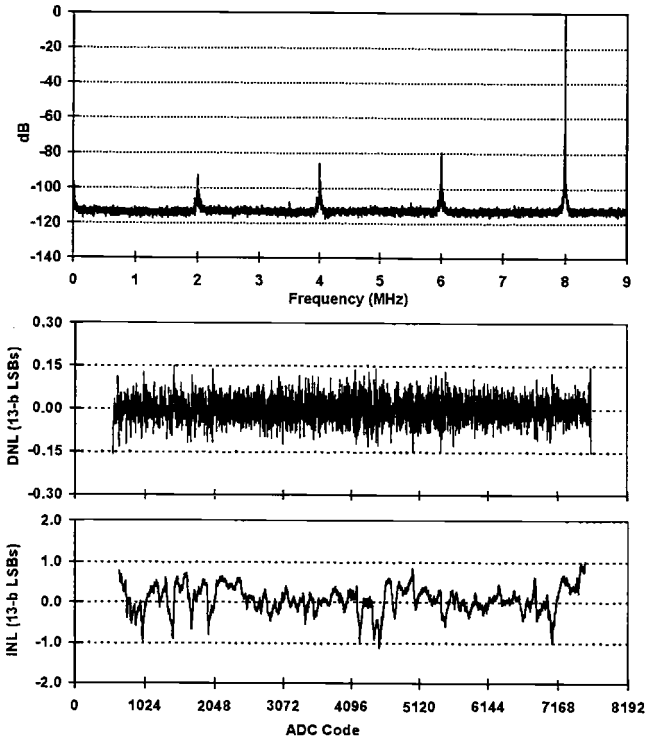
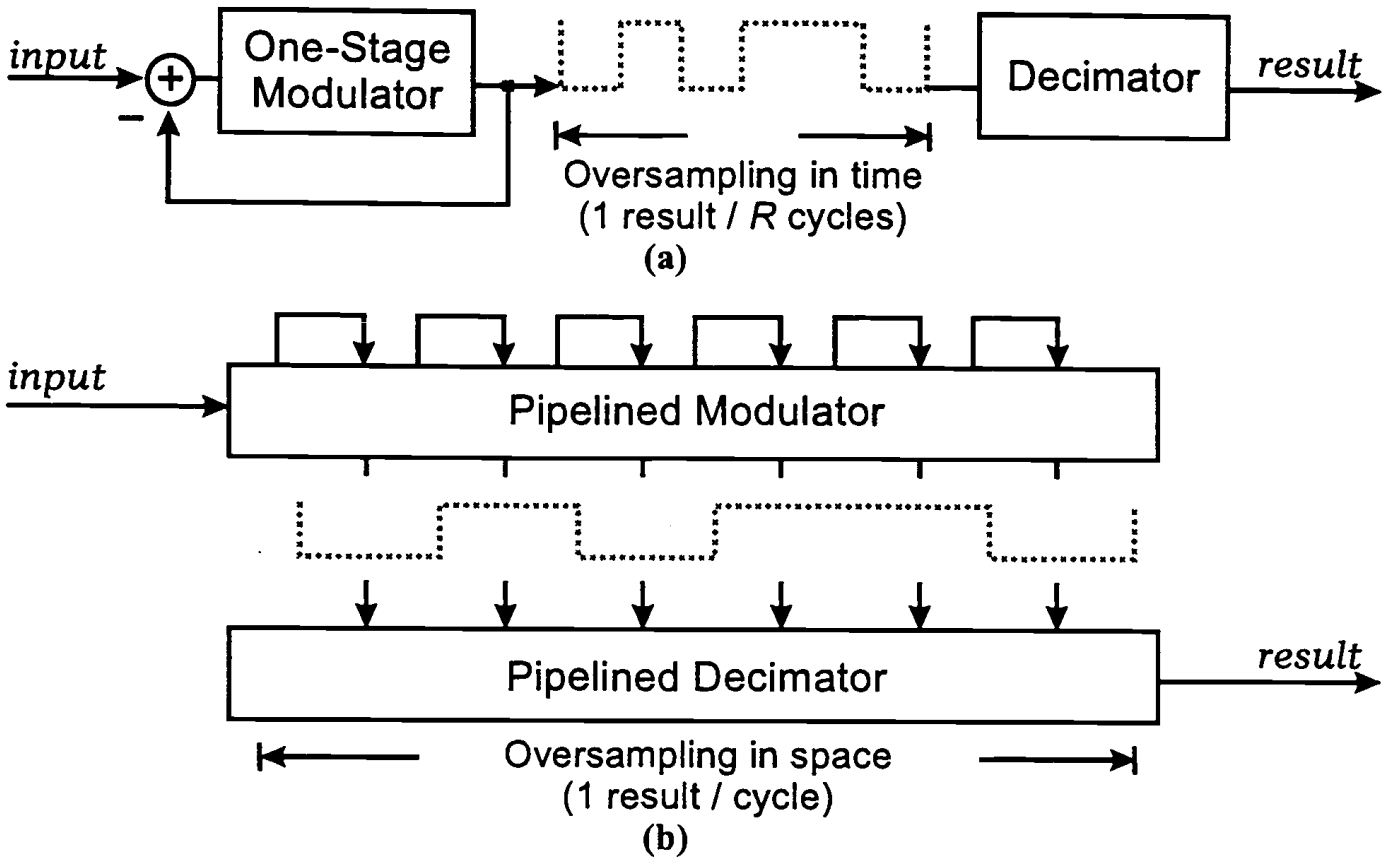


Figure 3.3.6. Measured spectral response, DNL, and INL at 18MSample/s, input near 8MHz.



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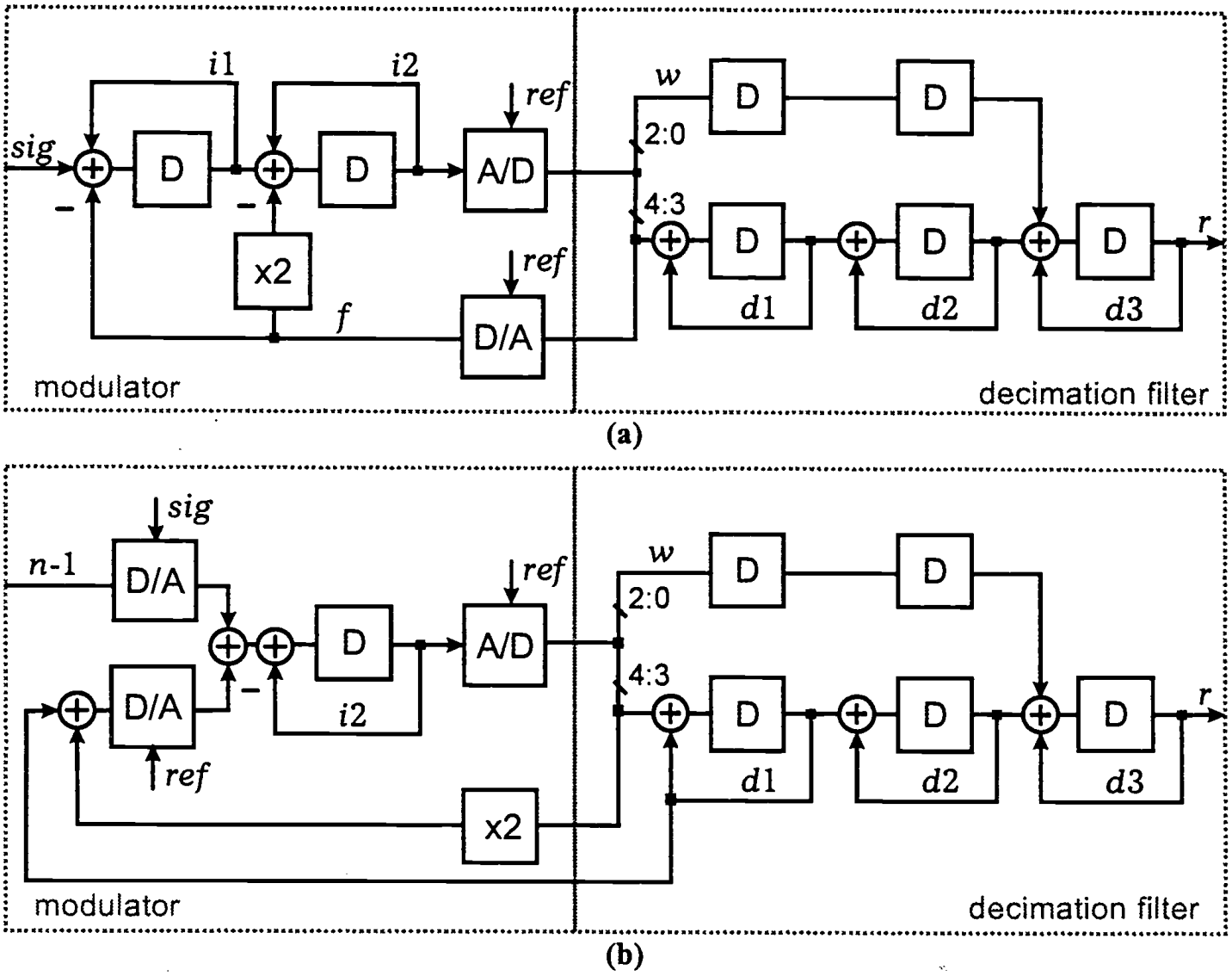

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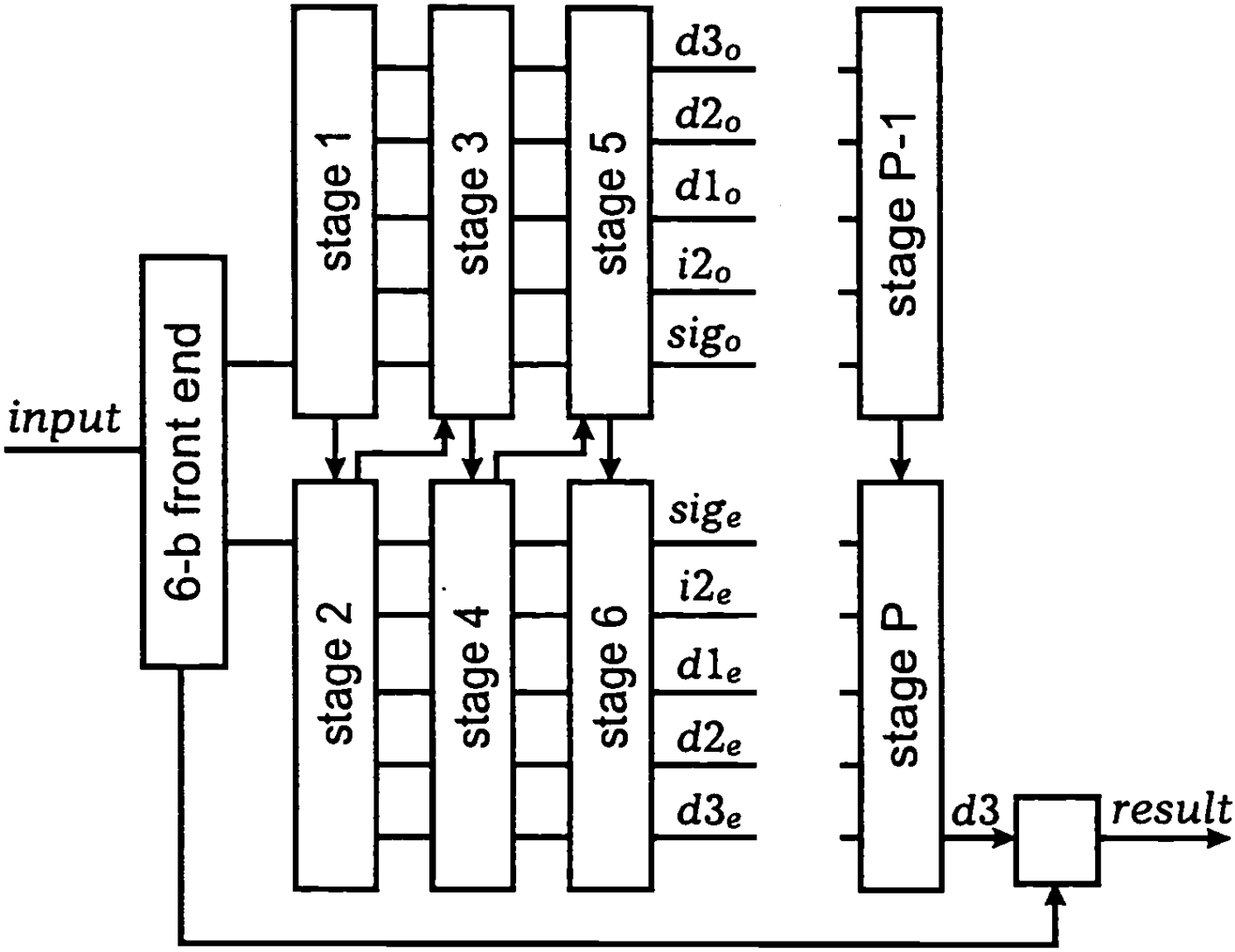

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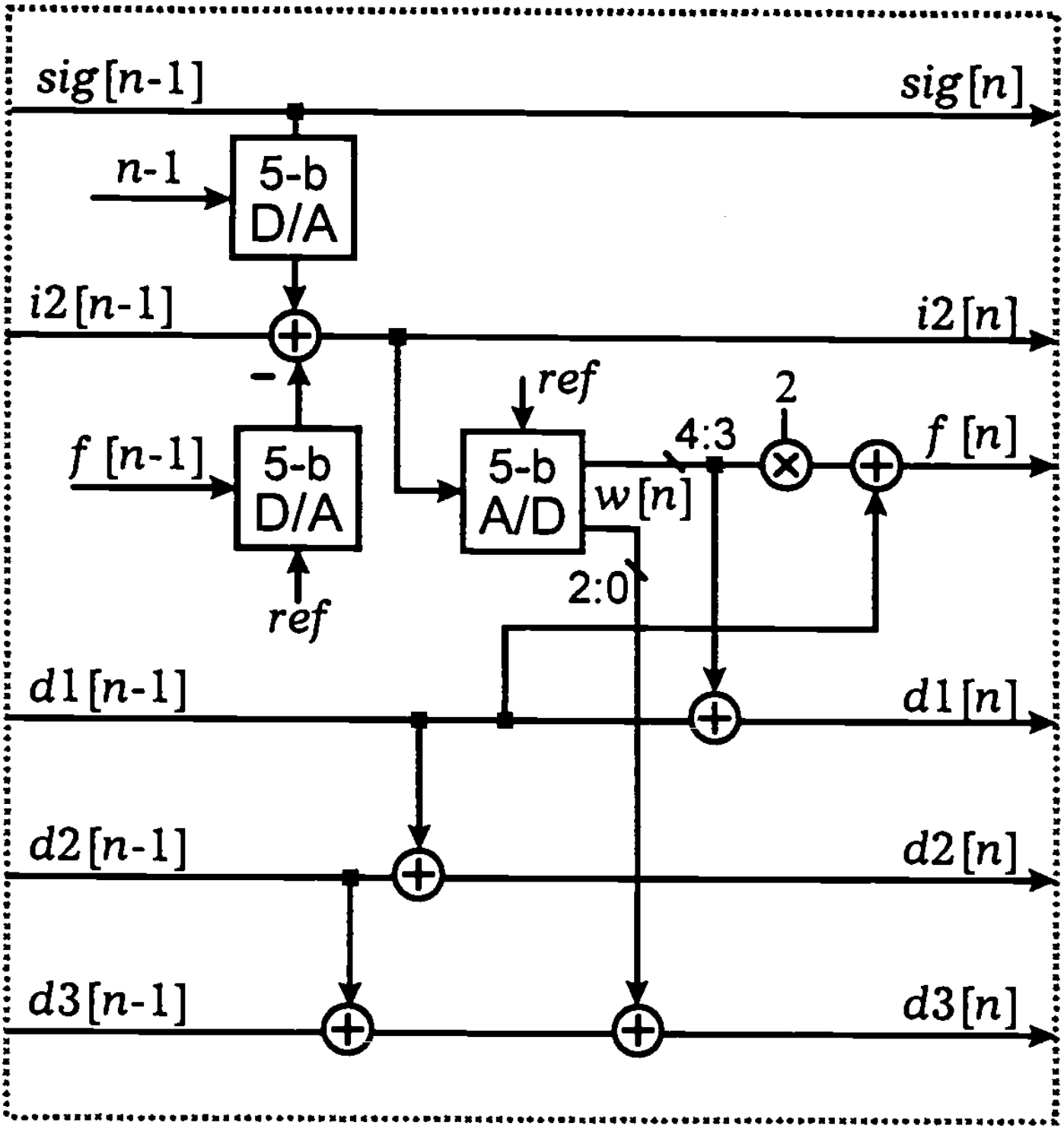

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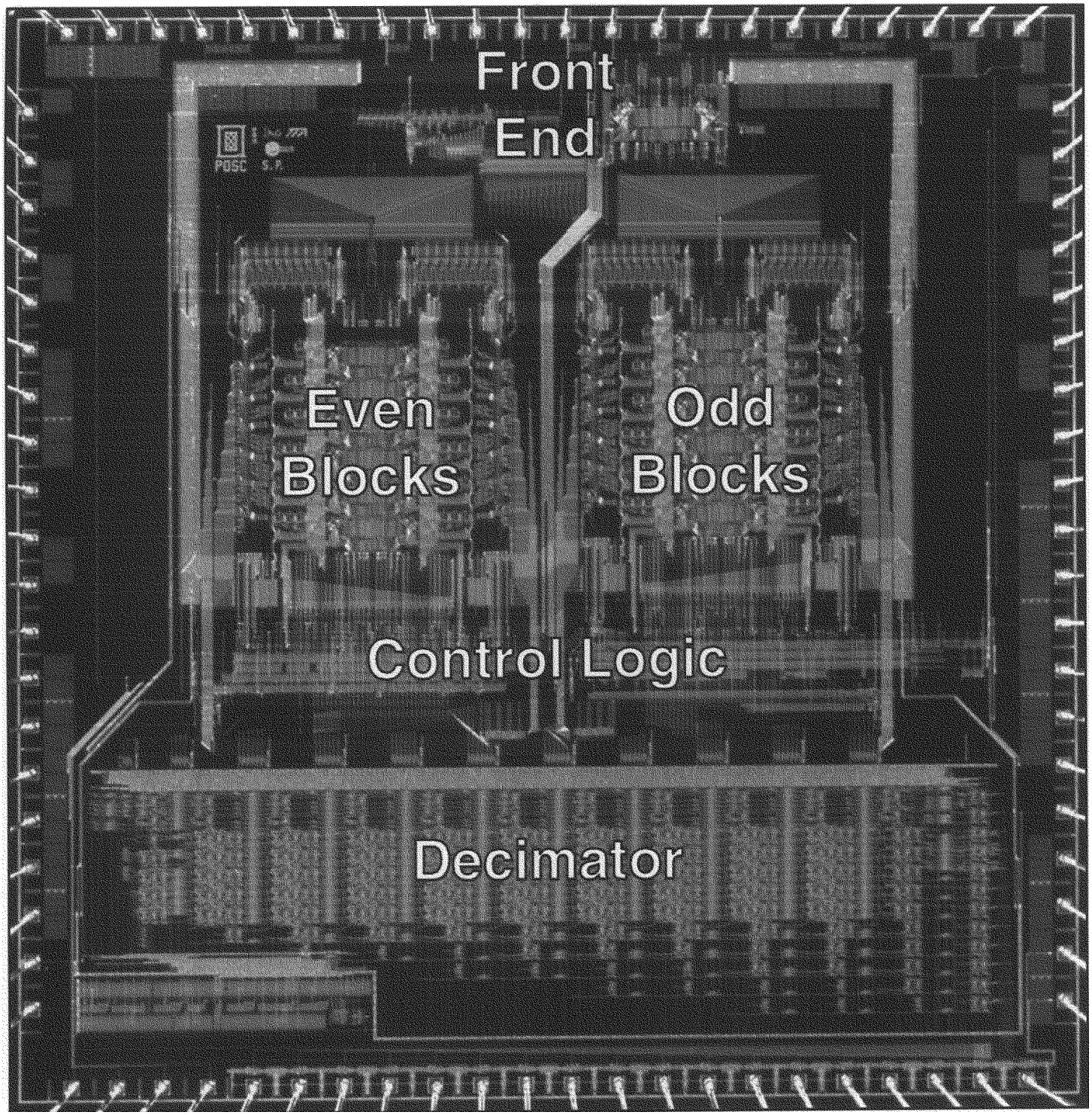

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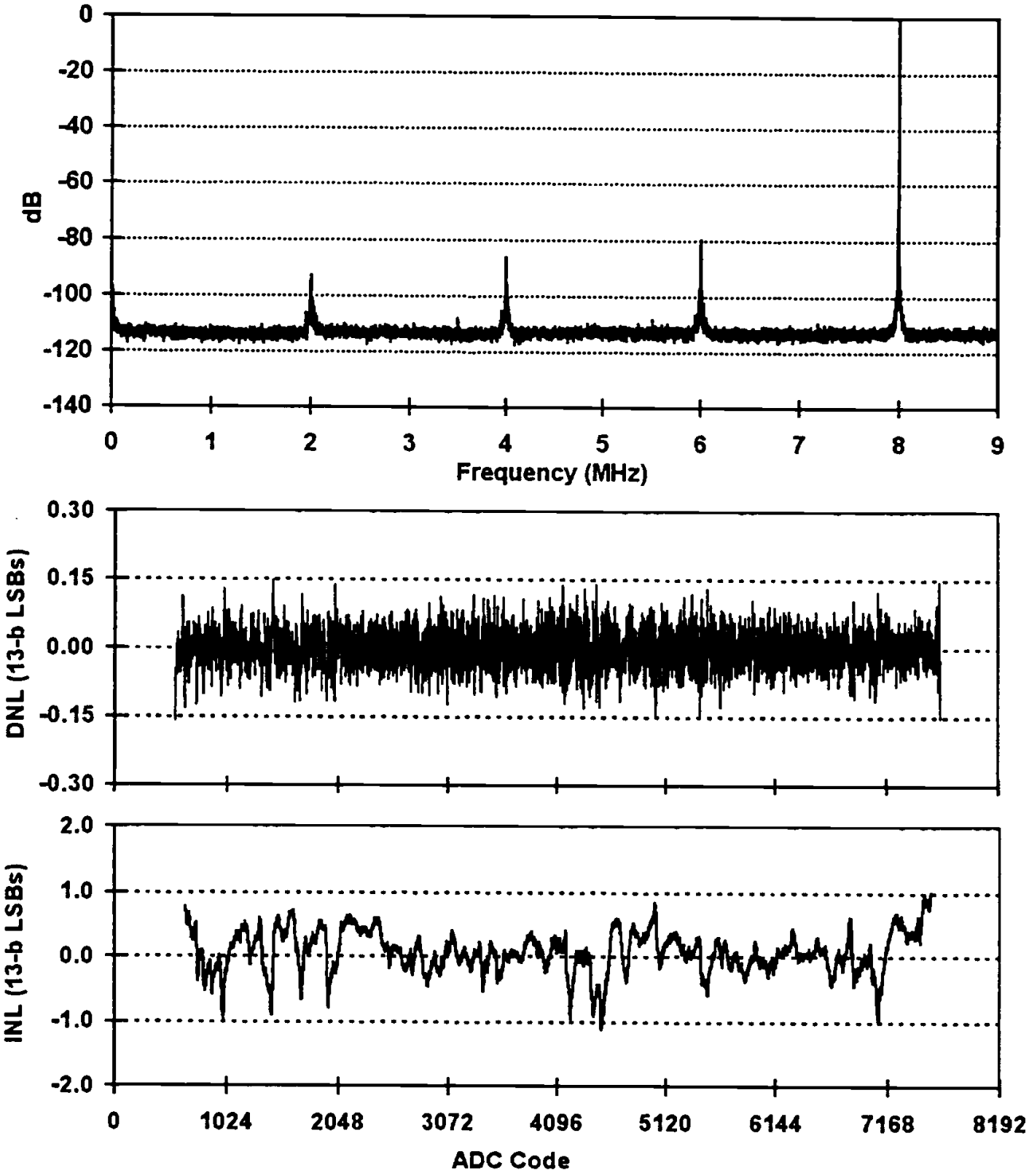

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