3.6 A Low-Power Reconfigurable Analog-to-Digital Converter

Kush Gulati and Hae-Seung Lee

Massachusetts Institute of Technology, Cambridge MA

There are applications that require ADCs that digitize signals at a wide range of bandwidth at varying resolution. Clearly, a conventional ADC with fixed topology and parameters cannot accomplish this task efficiently. An alternate approach is to employ an array of ADCs, each customized to work in narrow ranges of resolution and input bandwidth. Such a system would occupy a prohibitively large area to achieve optimal power consumption at fine granularity over bandwidth and resolution. A single ADC with reconfigurable parameters and reconfigurable topology would be able to achieve the above goal. Prior reconfigurable ADCs [1,2], however, have limited reconfigurability. This ADC provides a significantly larger reconfigurability space.

The concept of this ADC stems from the observation that certain ADC architectures such as the pipeline and ΣΔ ADC topologies are composed of the same basic components such as opamps, comparators, switches and capacitors. The difference between them, from a network perspective, is the interconnection between devices. Thus, a converter composed of these basic building blocks in conjunction with a configurable switch matrix, can adapt to these different topologies and work at different resolutions and bandwidths. Performance degradation due to switch parasitics is minimized by maximizing re-use of switches between different modes.

The reconfigurable ADC consists of several basic building blocks as shown in Figure 3.6.1a. The main reconfiguration logic utilizes a user-defined 'configuration-word' to determine the global structure of the ADC and the state of each block. The PLL shown in Figure 3.6.1a determines the appropriate bias current of the opamps. Each basic building block contains block reconfiguration logic that controls the static connection as well as the clocking of the switches. It also contains one opamp, the switch matrix, and a decision block. Reconfiguration of this ADC occurs at 3 levels: (1) architecture reconfiguration - involving the choice of either the pipeline or ΣΔ topologies. The ADC is in ΣΔ mode for resolution greater than 12b and in pipeline mode for lower resolutions. (2) resolution reconfiguration - in the pipeline mode, size of the capacitors and length of the pipeline can be modified while the ΣΔ relies on variation of oversampling ratio (OSR) to change resolution. Variation of the OSR at a fixed input bandwidth as well as the variation of the input bandwidth in either of the modes demands a method by which the power consumption of the ADC can track the sampling rate. (3) This is done through bandwidth reconfiguration – where a phase-locked loop (PLL) senses the clock frequency and varies the bias current of the opamps automatically.

To minimize ADC power consumption, consecutive stages of the pipeline mode ADC share the same opamp [3]. Overall offset of the ADC is corrected by chopping the ADC as a single block every clock cycle. Since each basic building block shown in Figure 3.6.1a contains one opamp, each block encapsulates 2 stages of the pipeline ADC. Additionally, consecutive blocks employ opamps and capacitors that are scaled with respect to the preceding block. An interstage scale factor of $1/2$ (inter-block scale factor of $1/4$) is selected to have a consecutive block thermal noise ratio of $1/4$. Figure 3.6.1b illustrates the resolution reconfiguring methodology in the pipeline ADC. A 12b mode pipeline employs blocks B1- B6, a 11b mode pipeline can tolerate twice as much thermal noise and employs blocks B2-B7, the 10b mode employs blocks B3-B7, and so on. An unused block is switched off. Thus a combination of shifting and truncating maintains kT/C limited operation and hence minimum power through varying resolution.

The ΣΔ mode utilizes a 4th-order cascade-of integrators with distributed feedback [4] and is embedded in blocks B1-B4, each block corresponding to a single integration. The offset and 1/f noise concerns in the ΣΔ are addressed by chopping the first block opamp so that additional switch parasitics cause minimal performance reduction in the pipeline mode.

Figures 3.6.2a and 3.6.2b show a typical differential-half switched-capacitor core in the pipeline and ΣΔ modes. The circuit that is active in a given mode is drawn in bold. Switches Sa and Sb determine the block input. C1 and C2 serve as the sampling and amplifying capacitors for the first stage in this block (odd stages in the pipeline) while C3 and C4 serve in the second stage in the block (even stage in the pipeline). The opamp employs a gain-enhanced telescopic topology and is shared between these 2 stages. In the ΣΔ mode, capacitors C1 and C2 are re-used to implement coefficients 'b' and 'a', respectively as illustrated in Figure 3.6.2c, while Cc and Cf implement the 'c' coefficient and the feedback capacitance, respectively. The clocking (Figure 3.6.2d) of the switches is in consideration of the differing charge injection concerns in the two different modes. Each block has 2 pairs of comparators to implement the 1.5b/stage digital error correction scheme. A variable-threshold comparator implements either ±Vref/4 thresholds (used in all but last stage of pipeline mode) or zero threshold (used in last stage of both modes).

Figure 3.6.3a shows the PLL employed for bandwidth reconfiguration. The VCO in Figure 3.6.3b is constructed from 3 scaled-down ADC opamp replicas such that the VCO frequency is proportional to the unity-gain frequency of these opamps. The charge-pump controls oscillation frequency via the VCO opamp bias currents. The same bias current is also fed to the opamps in the main ADC. The ADC clock is supplied to the input of the PLL. During locked conditions, the VCO oscillation frequency matches the clock frequency, fixing the bias currents of the ADC opamps. Thus, the settling time of the ADC opamps is matched to the ADC clock.

The ADC is fabricated in a TSMC 0.6μm DPTM CMOS process and occupies 10.5x7.6mm² die area. The reconfigurable ADC intrinsically requires an area slightly larger than a 12b ADC, however, the prototype layout is optimized not for area but for testability. The resolution of the ADC can be varied from 6 to 15b while bias current can be varied over about 3 orders of magnitude (Figure 3.6.5c) corresponding to a sampling rate range of 20kHz to 20MHz. Figure 3.6.4a shows the FFT of the ADC output in the 15b ΣΔ mode. Measured variation of SNR versus ADC analog power levels obtained by varying clock frequency for a fixed input bandwidth is shown in Figure 3.6.4b. Figures 3.6.5a and 3.6.5b show the measured non-linearity of the ADC in pipeline mode. Although the chip is designed for a maximum of 12b in pipeline mode, the measured INL and DNL exceeds ±1LSB due to mismatch among the small capacitors used. Standard digital calibration [5], which is not implemented on this chip for simplicity, would correct this problem. Figure 3.6.6 provides a summary of measured results.

Acknowledgements:
This research was funded by DARPA under agreement DAAL-01-95-K-3526, Center for Integrated Circuits and Systems, and a fellowship from Maxim Integrated Products. The authors thank C.G. Sodini, A. Shabra and M. Peng of MIT, T. Tewksbury, B.J. McCarrol and A.N. Karanicolas of Maxim Integrated Products, B.P. Brandt and D. Boisvert of National Semiconductor and P. Ferguson, T. Barber and S. Ho of Analog Devices for technical assistance.

References:

[1] US Patent No. US05691720, "Delta sigma analog-to-digital converter having programmable resolution/bias current circuitry and method," Nov. 25, 1997.
[2] Texas Instruments' TLV1562 Datasheet (www.ti.com/sc/docs/products/analog/tlv1562.html).
[3] K. Nagaraj, "A 250-mW, 8-b, 52-Msamples/s parallel-pipelined A/D converter with reduced number of amplifiers," IEEE J. of Solid Circuits, Vol. SC-32, No. 3, pp. 312-320, March 1997.
[4] S.A. Jantzi, W.M. Snelgrove and P.F. Ferguson, "A Fourth-Order Bandpass Sigma-Delta Modulator," IEEE J. of Solid-State Circuits, Vol. SC-28, No. 3, pp. 282-291, March 1993.
[5] H.-S. Lee, "A 12-b 600ks/s Digitally Self-Calibrated Pipelined Algorithmic ADC," IEEE J. of Solid-State Circuits, Vol. SC-29, No. 4, pp. 509, April 1994.

0-7803-6608-5/$10.00 ©2001 IEEE

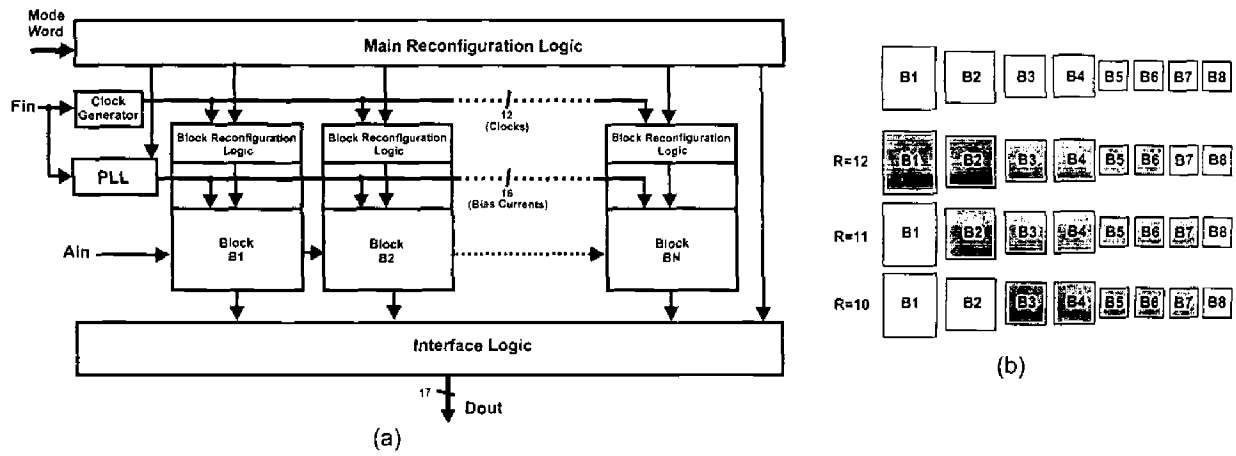


Figure 3.6.1: (a) Reconfigurable ADC block diagram. (b) ADC reconfiguring methodology.

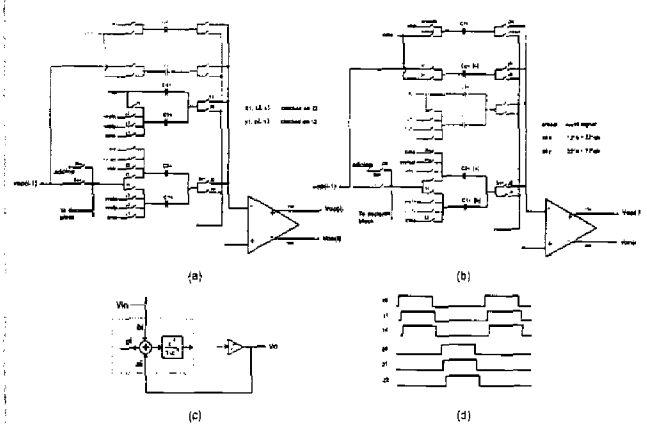


Figure 3.6.2: Switched-capacitor core in (a) pipeline mode, (b) ΣΔ mode, (c) Stage showing coefficients, (d) Clock diagram.

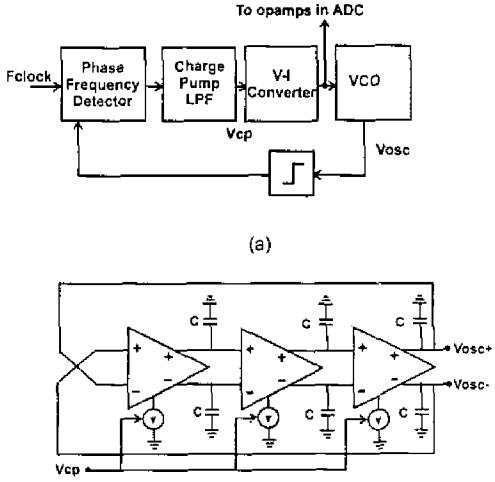
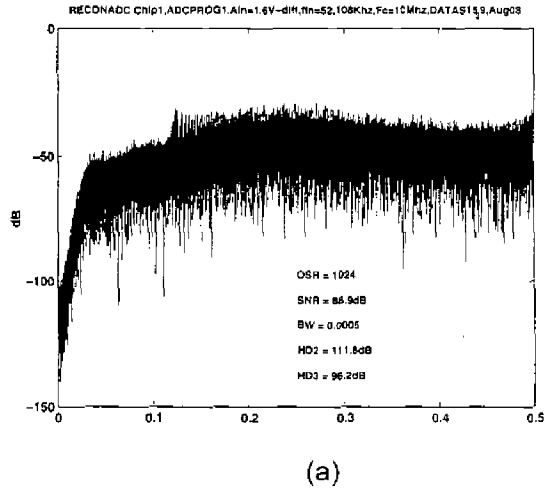


Figure 3.6.3: (a) PLL block diagram, (b) VCO conceptual diagram.



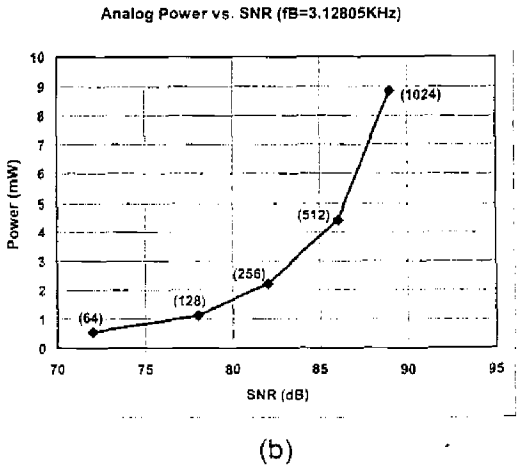


Figure 3.6.4: (a) FFT of ΣΔ output for fs=10MHz, OSR of 1024 and fin=3.13KHz.
(b) Measured variation of SNR versus OSR at fixed input bandwidth. The number in parenthesis is the OSR.

Continued on Page 429

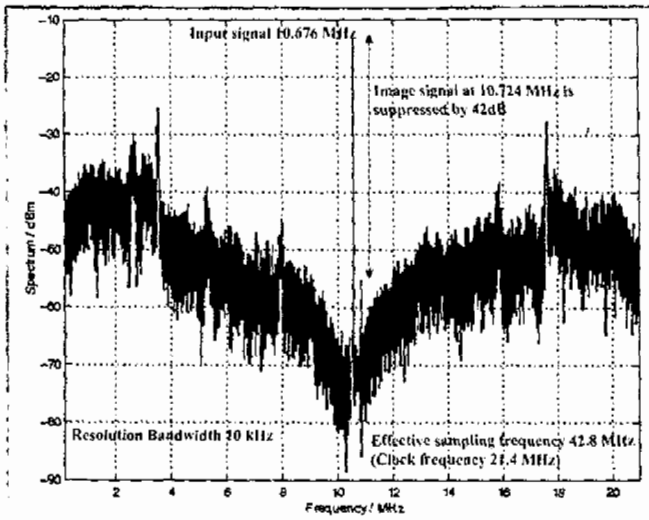


Figure 3.5.6: Measured output spectrum of the second-order SO bandpass ΣΔ modulator.

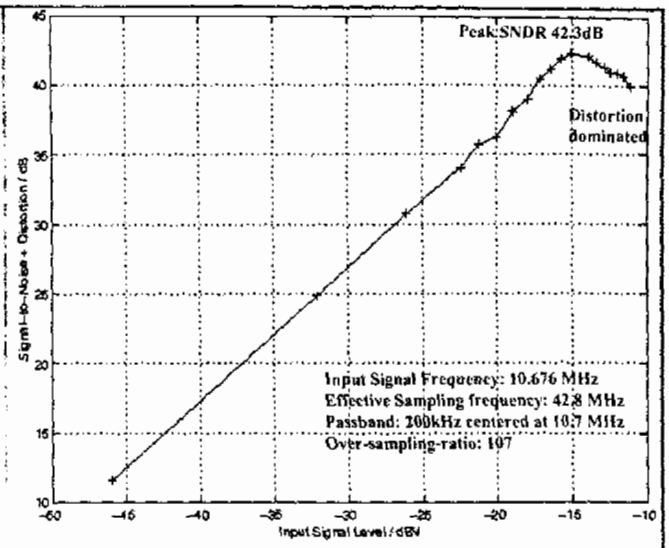
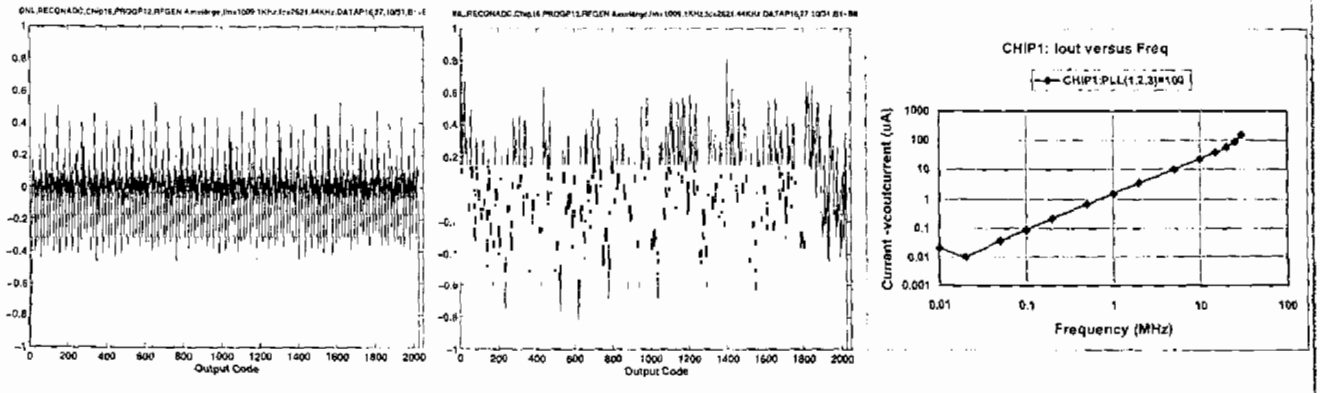


Figure 3.5.7: Measured SNDR vs. input signal level.



(a) (b) (c)

Figure 3.6.5: Measured (a) DNL and (b) INL plots for ADC in pipeline mode (fin=1MHz and Fc=2.62KHz and Fc=2.62KHz); LSB corresponds to 11 bit levels. (c) Typical measured variation of bias current generated by PLL with changing clock frequency.

Process	0.6μm CMOS, DPTM
Die Area	10.6mm x 7.6mm
Power Supply	2.7V-4.6V
Parameter Reconfiguring Time	12 clock cycles
Sigma-Delta 15 Mode (3.3V)	
Resolution	15 bits
Fclock	10MHz
Fin	3.13KHz (1.5V p-p differential)
OSR	1024
Power	8.8mW
HD2	111.8dB
HD3	96.21dB
Pipeline 12 bit Mode (3.3V)	
Resolution	11 bits
Fclock	2.62MHz
Fin	1MHz (1V p-p differential)
Power	24.6mW
DNL	< +/- 0.55 LSB
INL	< +/- 0.82 LSB

Figure 3.6.6: Measured performance at 25°C.

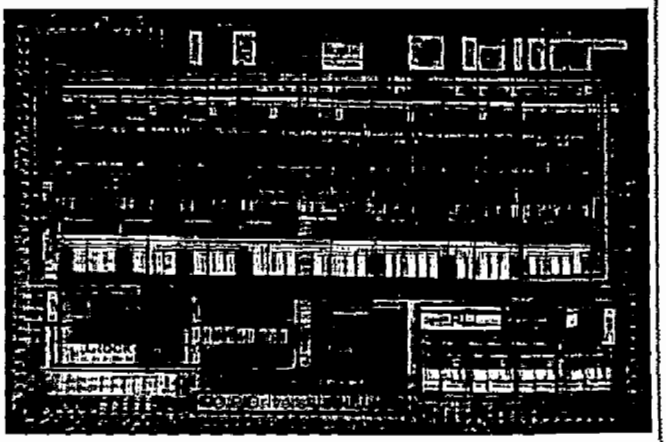


Figure 3.6.7: ADC micrograph.